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Engineering Specification

INTERLOCK BEAM POSITION MONITORS FOR THE LHC BEAM DUMPING SYSTEM

Abstract

A total of 8 Beam Position Monitors BPMs are required in IR6 for the LHC beam dump system. These monitors are connected to the Beam Interlock System BIS and ensure that the amplitude of the orbit in IR6 does not exceed 4 mm. The system will use standard LHC BPM front-end electronics but will run with a special firmware version downloaded to the digital acquisition FPGA.

This document describes the Interlock BPM System and its connections to other machine systems. It specifies the requirement for the logic in the firmware for the front-end FPGA, defining the tolerances for the beam dump trigger in terms of the position thresholds and the numbers of bunches out of tolerance as a function of the number of turns considered. Data diagnostic requirements for Post-Operational Checks, logging and post-mortem are also identified.

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History of Changes

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1. SCOPE OF THIS SPECIFICATION

A total of 8 Beam Position Monitors BPMs are required in IR6 for the LHC beam dump system (LBDS). These monitors are connected to the beam Interlock System BIS and ensure that the amplitude of the maximum orbit in IR6 at the moment of extraction does not exceed 4 mm. The FPGAs on the front-end electronics will implement specific logic allowing the end-users to define the tolerances for the beam dump trigger, in terms of the position thresholds and the numbers of bunches out of tolerance as a function of the number of turns considered. This document:

- describes briefly the architecture of the Interlock BPMs and the links to the BIS and the control system;
- specifies the conditions for the generation of the beam dump trigger signal;
- describes the different data diagnostic functionalities required.

2. LBDS INTERLOCK BPMs

To ensure that the orbit at the extraction septum MSD remains below 4 mm, a total of 8 warm strip-line BPMs, with two variants (BPMSA and BPMSB) are installed, 2 per beam at the Q4 and Q5, on either side of point 6 (see Table 1). These will acquire both vertical and horizontal positions on an auto-triggered basis (bunch-by-bunch), such that the system does not rely on machine timing. The monitors are connected to Digital Acquisition Boards (DAB64x), installed in 2 VME chassis (CFV-SR6-BPMINT1 & CFV-SR6-BPMINT2) and connected as shown in Figure 1. One BPM from L6 and one BPM from R6 for both beam1 and beam 2 are to be processed in each interlock VME crate. A separate VME board in each crate will regroup the interlock from each plane of each BPM and generate the final interlock status for the BIC system.

Monitor	S [m]	Type	Electrode Type	BPM Diameter (mm)	Location
BPMSB.B4L6.B2	16518.055	BPMSB	120mm stripline	131	RA63
BPMSB.A4L6.B2	16518.690	BPMSB	120mm stripline	131	RA63
BPMSA.B4L6.B1	16519.275	BPMSA	120mm stripline	81	RA63
BPMSA.A4L6.B1	16519.860	BPMSA	120mm stripline	81	RA63
BPMSA.A4R6.B2	16803.745	BPMSA	120mm stripline	81	RA67
BPMSA.B4R6.B2	16804.330	BPMSA	120mm stripline	81	RA67
BPMSB.A4R6.B1	16804.915	BPMSB	120mm stripline	131	RA67
BPMSB.B4R6.B1	16805.550	BPMSB	120mm stripline	131	RA67

Table 1. Positions and types of LBDS Interlock BPMs in IR6.

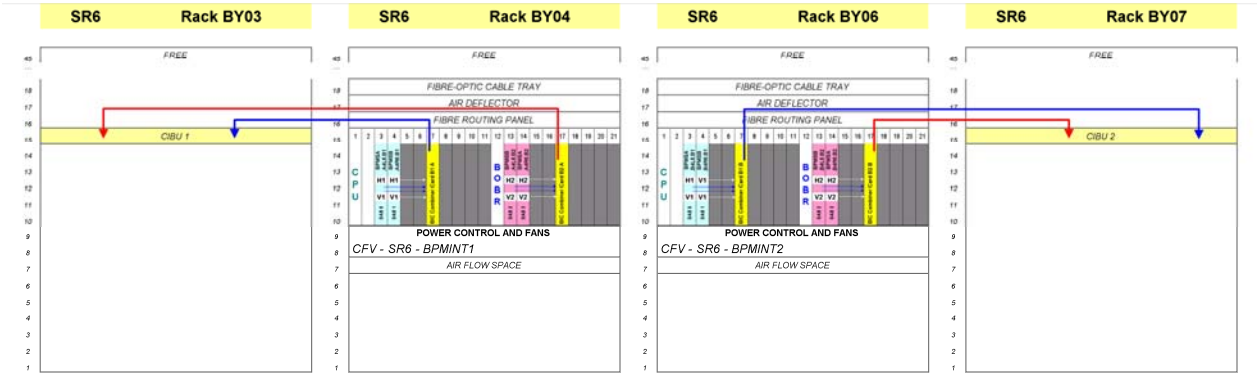

Figure 1 – VME and CIBU layout in SR6

3. INTERLOCK TRIGGER CONDITIONS

The bunch position acquisition will be made on a bunch-by-bunch, turn-by-turn basis. The algorithm to decide whether to trigger the beam dump must reliably dump the beam when the orbit is outside tolerance, while restricting to a minimum the number of spurious beam dumps. To enable a compromise between safety and availability to be realised, it is proposed that the parameters in the comparison algorithm be configurable using the Critical Settings Management (MCS) system.

It is proposed that an internal clock in the front-end FPGA triggers checks on a virtual turn basis, with a time interval of ~ 89 μs. This will not be synchronised to the LHC revolution frequency, and may therefore differ by a small amount from the actual revolution time. This will make the system more robust, allowing it to run independently of the bunch synchronous timing used for all other BPM acquisitions.

The system requires the following parameters, all of which should be defined as 'critical' and managed by the MCS system:

1. $+X_{max}$, $-X_{max}$, $+Y_{max}$ and $-Y_{max}$ for the actual DUMP position thresholds (nominally 3.5 mm). These will be entered into the FPGA by the FESA front-end as four 10-bit ADC numbers corresponding to these limits after taking into account the calibration factors linked to the BPM geometry and electronics.
2. $+X_{alarm}$, $-X_{alarm}$, $+Y_{alarm}$ and $-Y_{alarm}$ for the ALARM position thresholds. An internal consistency check shall be implemented to ensure that the alarm thresholds are always inferior to the dump thresholds described in 1).
3. T_1 and T_2 define the length of the two possible time windows expressed in number of turns.
4. BD_1 and BD_2 which define the maximum number of bunches which may be outside the position threshold defined in 1) or 2) within the corresponding time window defined in 3) before a dump or alarm is triggered.
5. The BPM scale factor (Kf) and calibration factors (HCalLow, HCalMid, HCalHigh, VCalLow, VCalMid, VCalHigh) used to convert the dump thresholds in mm to raw ADC values for the front-end FPGA.

Two internal variables per monitor, N_{1max} and N_{2max} , shall be used to count the number of bunches within the past T_1 and T_2 turns respectively which exceed $+X_{max}$, $-X_{max}$, $+Y_{max}$ or $-Y_{max}$. The interlock should be triggered if $N_{1max} > BD_1$ or $N_{2max} > BD_2$.

A further two variables, N_{1alarm} and N_{2alarm} , shall be used to count the number of bunches within the past T_1 and T_2 turns which exceed $+X_{alarm}$, $-X_{alarm}$, $+Y_{alarm}$ or $-Y_{alarm}$. The alarm should be generated if $N_{1alarm} > BD_1$ or if $N_{2alarm} > BD_2$. This alarm shall be transmitted to the LASER alarm screen.

This approach allows the definition of two time windows with different characteristics. It is envisaged to have the first condition look at a small number of bunches, over a larger number of turns (for example 4 bunches out of tolerance for 20 turns), while the second condition can check a larger number of bunches for a smaller number of turns (for example 20 bunches in 2 turns). It is hoped that this approach will reduce the number of false dump triggers arising from any spurious acquisitions, while still reacting in time to potentially dangerous conditions.

The LHC BPM system works in one of two possible sensitivity settings. In the HIGH sensitivity setting the system will see all bunch intensities from 2×10^9 charges upwards. However, for intensities higher than $\sim5\times10^{10}$ charges the system starts to become sensitive to any small electronic reflections in the BPM cabling, which can often lead to spurious position readings. Above such intensities it is therefore usual to switch to the

LOW sensitivity setting, which makes the system blind to any bunches with less than ~ 2×10^{10} charges.

A surveillance process shall be put in place to ensure that the front-end electronics for all BPMs for a given beam uses the correct sensitivity setting.

4. DATA DIAGNOSTIC FUNCTIONALITIES

The internal variables and parameters must be readable via the FESA class for the monitors. These values may be required for checks e.g. by the sequencer and software interlocking systems.

The interlock BPMs shall provide general orbit data via UDP to the feedback controller. This will allow these monitors to be displayed as standard BPMs in the LHC orbit GUI.

The Interlock BPMs shall provide the conventional post-mortem buffer, with data to be pushed to the post-mortem server on receipt of the PM request timing event.

An additional Interlock BPM Post Mortem buffer shall store the $N_{1max,2max,1alarm,2alarm}$ registers along with the maximum and minimum positions reached for the last 1000 turns. This will allow the evolution of system prior to any requested beam dump to be analysed.

The interlock firmware shall implement an internal counter to allow regular checks on the operational status of the routine.

The system shall provide an alarm to the LASER alarm screen whenever $N_{1alarm} > BD_1$ or $N_{2alarm} > BD_2$.

5. CONNECTION TO THE BIC SYSTEM

Each interlock BPM shall be able to generate independent, out of limit hardware signals for the horizontal and vertical plane. These hardware signals shall be regrouped locally to provide 1 CIBU signal for beam1 and 1 CIBU signal for beam2 from each VME crate. The VME combiner card shall be able to determine which input caused a dump to occur.

The interlock signal must always be set FALSE whenever the interlock conditions described in 3 above are out of tolerance.

The inputs to the BICs must be ‘maskable’ to allow setting up of the extraction and its protection devices with safe beam.

It shall be possible to generate a request for a dump via software to allow a full test of BIS connectivity.

6. FAILSAFE AND STARTUP BEHAVIOUR

When the BPM crate is off the interlock signal must be FALSE.

The crate should ideally start up with the last valid set of parameters and interlock thresholds – but since a reset by the control system or sequencer will be required, and a check must anyway be made of the validity of the parameters, these values could systematically be loaded in from the control system via MCS using e.g. the sequencer.