

## Functional Specification

# REQUIREMENTS FOR THE FAST MMAGNET CURRENT CHANGE MONITORS (FMCM) IN THE LHC AND THE SPS-LHC TRANSFER LINES

### *Abstract*

Fast Magnet Current Change Monitors (FMCM), initially developed at DESY for the HERA storage ring, will be deployed in the LHC and the SPS-LHC-CNGS transfer lines [1]. The system interfaces directly to the beam interlock systems of the LHC and the SPS-LHC-CNGS transfer lines and issues beam dump requests or inhibits extraction in case of powering failures that would have fast effects on the particle beam(s). The document summarizes the requirements in terms of hardware and functionality.

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## 1. INTRODUCTION

The need for additional protection measures to be applied to a number of electrical circuits in the SPS-LHC transfer lines and the LHC to protect against fast beam losses in case of powering failures has been discussed for some time [2] [4]. The need for such monitors has been illustrated by the beam incident in TT40 end of 2004 (the monitor would have prevented the accident) [3]. Installation of such monitor has been recommended by the reviewers during the Review on LHC Machine Protection in April 2005 [5].

A Fast Magnet Current Change Monitor (hereafter referred to as FMCM) detects powering failures in critical electrical circuits and provides a permit signal to the beam interlock system in the transfer lines or the LHC. Such system is operating successfully at HERA [6], and a series of tests have recently shown that the monitors fully comply with the requirements for the CERN accelerators.

## 2. FUNCTIONAL DESCRIPTION

Based on the voltage measured across the magnet or circuit with an external voltage divider box and an isolation amplifier box, the monitor performs a real time calculation of the magnet current, using a low pass filter. This signal then passes a high pass filter to amplify the fast current changes, typical during a powering failure of the circuit. These fast current changes are fed to a comparator to detect if they are inside a tolerance window. The tolerance window (absolute tolerance with respect to the maximum circuit current; symmetric around zero) is being defined by a front panel potentiometer and an extraction inhibit/beam dump is initiated in case the upper or lower threshold is exceeded. It is important to understand that the FMCM will only detect fast changes relative to the last millisecond. Slow changes of the absolute current value have to be detected by other systems (converter controls, fast extraction interlocks), that have to verify the absolute value at least every 5 ms.

The FMCM is connected to the beam interlock system using a standard user interface (CIBU-Box). A minimum/maximum tracking is included to easily identify the correct thresholds during commissioning and to verify if the thresholds are set correctly and not affected by other effects during operation, e.g. electromagnetic noise. A post mortem buffer records magnet voltage, calculated magnet current changes, the measured DCCT current changes and the voltage of the 'U\_ext' input in case of an alarm. The values are recorded in the time range of approx. 30ms before the alarm, until 10ms after an alarm with a resolution of approx. 21 $\mu$ s in time and 12 bits for the amplitude (for the LHC the recording time is doubled, while the resolution is only 42  $\mu$ s). Only the last event is recorded in this buffer, along with the UTC timestamp of the occurred event.

The following table summarizes the main parameters of the FMCM:

**Size:** 19 inches wide standalone module, 1U high (44 mm)

**Power supply:** internal power supply (non-redundant)

**Main PCB:** analogue part for signal processing and FPGA for Post Mortem (PM) recording and the RS422 interface for data readout and remote control of the FMCM

**Main Inputs:**

- 6-pole LEMO connector to connect the magnet voltage
- 2-pole LEMO connector to connect a DCCT (for post mortem recording)
- 2-pole LEMO connector to connect a voltage 0..10V to be included in the post mortem buffering (spare channel)

**Main Outputs:**

- Burndy 8 pin, female connector to connect to the CIBU-Box

**Other Inputs / Outputs:**

- 9 pin female D-sub connector for the RS 422 connection of the system to the CERN control system
- 1-pole BNC (LEMO) connectors for timing connection and for PM triggering



Figure 1: DESY version of the Fast Magnet Current Change Monitor (before CERN adaptation; in the back the power supply and in the front part the analogue electronics and the FPGA)

**3. LAYOUT OF THE SYSTEM**

A number of electrical circuits in the transfer lines and the LHC should be equipped with an FMCM. This includes normal conducting separation dipoles in IR1 and IR5 of the LHC, injection and dump septa magnets in IR2, IR6 and IR8 and magnets in the collimation insertions IR3 and IR7. In these insertions failures such as mains failures could affect a large numbers of normal conducting magnets at the same time. In the transfer lines systems are installed for the septa magnets, main bends and switching magnets.

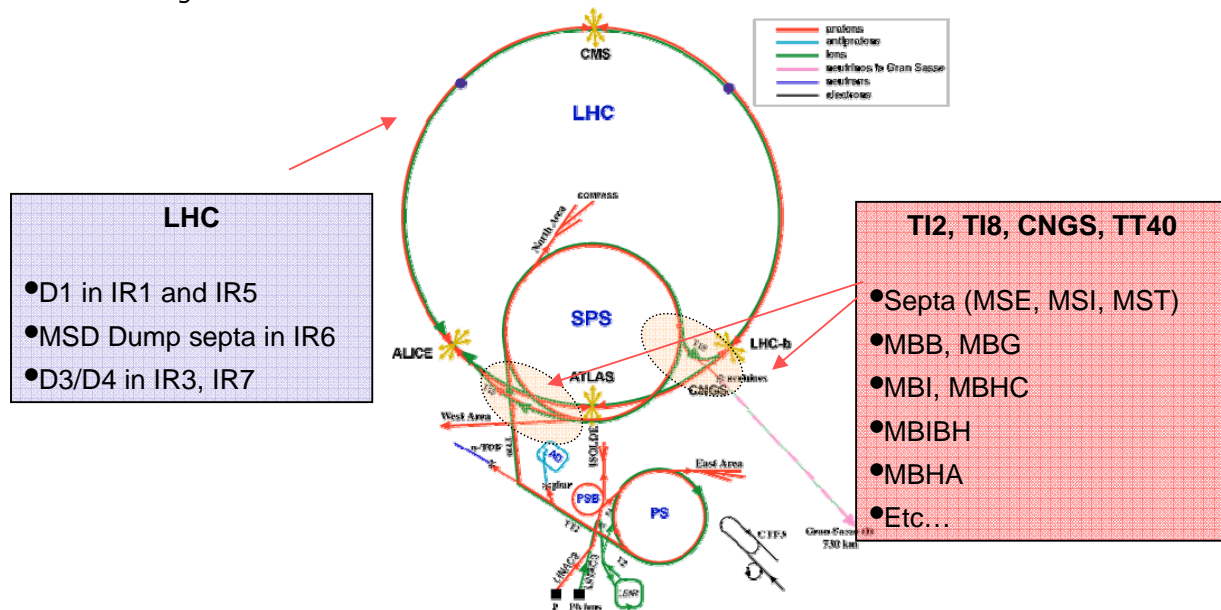


Figure 2: Layout of the FMCM and the foreseen installation locations in the LHC and the SPS-LHC Transfer lines

Due to the nature of the electrical circuits to be protected at CERN, there will be two different configurations for the FMCM:

1. **Slow ramping magnets:** This group includes all LHC magnets which only follow slow ramps during the energy ramp.
2. **Fast ramping magnets:** These magnets include all transfer line magnets (SPS extraction and LHC injection septas, main dipoles, dipole correctors and magnet switched) which are ramped up before extraction starts, remain at nominal current for the following extraction and are ramped down again until the next extraction (cycling lasts in between 6 and 20 seconds depending on the cycle mode of the SPS). There will be 3 different cycles for fast ramping magnets. A cycle for TI8/TI2 magnets, a cycle for CNGS extractions and a special CNGS cycle for the MBG 4101M circuit (due to cooling constraints and a limit for the Irms) as shown in Figure 3. Extractions will take place roughly 20ms before the ramp down, i.e. at 480ms after reaching the flat top. In case of the CNGS cycle, two consecutive extractions will take place at 430ms and 480ms after reaching the flat top. The FMCM installed on fast ramping magnets will only provide an extraction window once the current at flat top is within the tolerance window. The post-mortem readout needs to be adapted to this event series in order not to lose valuable data.

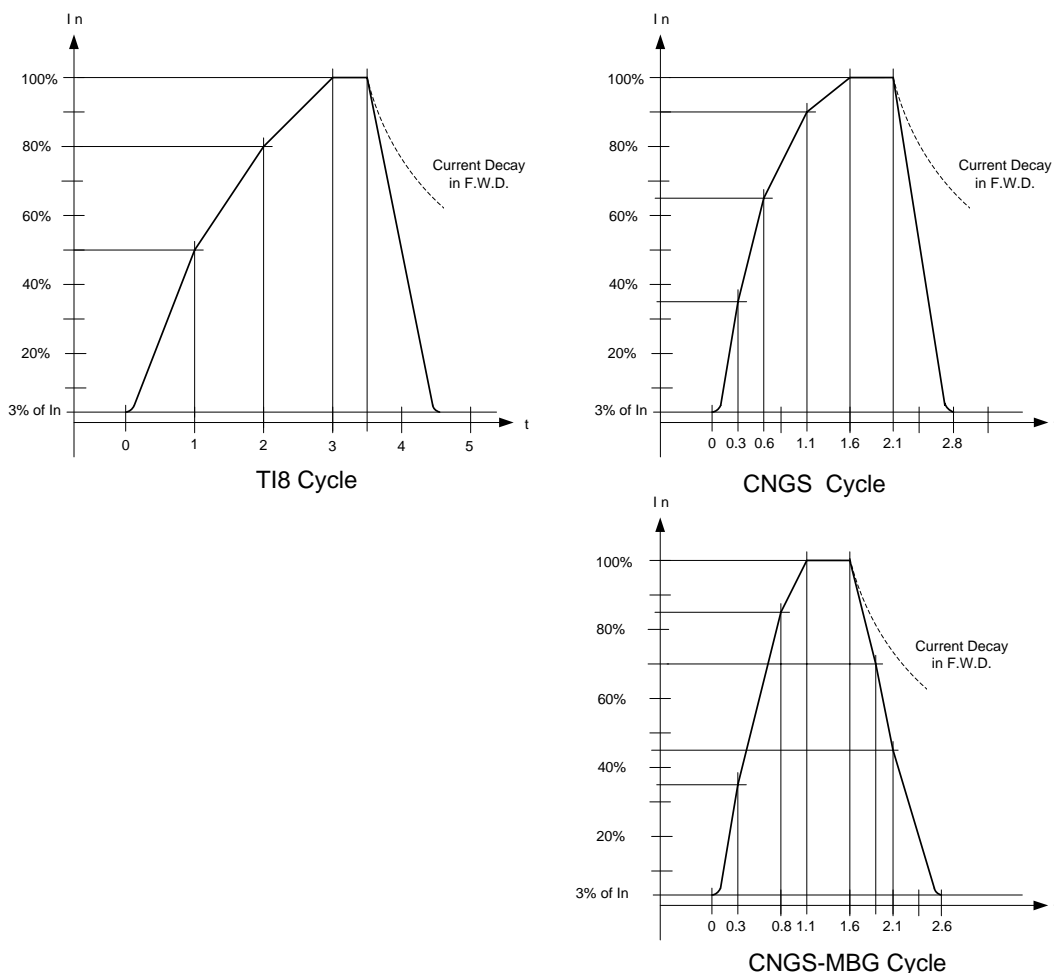


Figure 3: Extraction cycles for CNGS and LHC beam

### 3.1 INSTALLATION OF SYSTEMS IN THE TRANSFER LINES

For the SPS-LHC-CNGS transfer lines 14 monitors need to be installed. Installation of the FMCM (1U) and the CIBU interface (2U) will take place in the corresponding power converter. The controls interface will be provided by a VIP626 card, providing along with its mezzanine card a total of eight RS422 interfaces, sufficient to cover the necessary installations of FMCM in each of the 5 surface buildings (BA4, BB4, SR8, BA6 and SR2). This card will be installed in the controls rack (ROCS-Mugef; Research Operational Controls Structure – Multi generator functions) of the power converters (see also Appendix #1).

The following electrical circuits in the transfer lines between SPS and LHC/CNGS will be equipped with a FMCM (details on the electrical parameters can be found in Appendix #3):

Converter Name	Location	Control ROCS	Transfer Line	BIC (loc.)
MSE	BB4	M1SBB4	TT40	TT40 (BA4)
MBHC 4001M	BA4	M1SBA4	TT40	TT40 (BA4)
MBHA 4003M	BA4	M1SBA4	TT40	TT40 (BA4)
MBSG 4100M	BB4	M1SBB4	TI8/ CNGS	TT41 (BA4)
MBG 4101M*	BA4	M1SBB4	CNGS	TT41 (BA4)
MBI 8160M*	BA4	M1SBA4	TI8	TI8up (BA4)
MBIAH 8783M	SR8	M1SSR8	TI8	TI8dw (SR8)
MSIB 8813M	SR8	M1SSR8	TI8	TI8dw/Inj (SR8)
MST 6177	BA6	M3SBA6	TT60	TI2up (BA6)
MSE 6183M	BA6	M3SBA6	TT60	TT60 (BA6)
MBB 2015M	SR2	M1SSR2	TI2	TT60 (BA6)
MBI 2213M	SR2	M1SSR2	TI2	TI2dw (SR2)
MBIBH 2931M	SR2	M1SSR2	TI2	TI2dw (SR2)
MSIB 2952M	SR2	M1SSR2	TI2	TI2dw/Inj (SR2)

Table 1: Monitors in the transfer lines (\*: using the same power supply and unlike other circuits not equipped with a free-wheeling diode)

### 3.2 INSTALLATION OF SYSTEMS IN THE LHC

Monitoring of the electrical circuits for normal conducting separation magnets in IR1 and IR5 is required, for septum magnets in the beam dump lines, and for the insertions with normal conducting dipole and quadrupole magnets in IR3 and IR7.

In addition to these 6 systems, another 4 to 10 systems might be required for the protection of the circuits with quadrupole magnets: RQ4.LR3/7, RQ5.LR3/7, RQT4.L3/7, RQT4.R3/7, RQT5.L3/7 and RQT5.R3/7.

The risk of having fast beam losses is enhanced if a powering failure leads to the trip of several power converters supplying the current for all magnets in a zone. Due to the large number of normal conducting circuit in IR3 and IR7, it might be envisaged to install monitors for the most critical electrical circuits. Circuits are more critical if they have a shorter time constant and a large impact on the beam.

Installation of the FMCM (1U) and the CIBU interface (2U) will take place in the rack of the according beam interlock controller of the LHC.

The following electrical circuits in the LHC will be equipped with a FMCM (details on the electrical parameters can be found in Appendix #3):

Converter name	Location	Control LHC	Area	BIC (loc.)
RD1.LR1	SR1	FGC	LHC	CIBC.L1 (US15)
RD1.LR5	SR5	FGC	LHC	CIBC.L5 (UJ56)
RMSD.LR6B1	SR6	FGC	LHC	CIBC.L6 (US67)
RMSD.LR6B2	SR6	FGC	LHC	CIBC.L6 (US67)
RD34.LR3	SR3	FGC	LHC	CIBC.L3 (SR3)
RD34.LR7	SR7	FGC	LHC	CIBC.L7 (SR7)

Table 2: Monitors for the LHC electrical circuits with dipole magnets

In case the BIC is in the same location as the power converter, the voltage across the magnets will be picked up at the power converter terminals (SR3 and SR7). In the other cases where power converters are in the surface buildings and the BIC is in the underground area, the voltage across the magnets is picked up at the magnet terminals.

As for the transfer lines, the controls interface will be provided by a VIP626 card, providing a total of eight RS422 interfaces which is sufficient to cover the necessary installations of FMCMs in the 5 surface buildings (SR1, SR3, SR5, SR6 and SR7). This interface card will be installed in the VME crate of the beam interlock controller (see also Appendix #1).

### 3.3 CONNECTIONS TO THE BEAM INTERLOCK CONTROLLER (BIC)

Each FMCM is to be connected to a (mask-able) BOTH BEAMS input of the nearest beam interlock controller in the LHC (in case of failure both beams will be dumped) or the beam interlock controller managing the corresponding transfer line, following the specification for the CIBU connection.

For the Permit A & B signals of this connector, the FMCM shall provide two independent switches as specified in the CIBU specification. For the commissioning of this input, the FMCM shall be able to provoke individual inhibit/beam dump signals on request. However, the FMCM must never be able to disable the dump request towards the BIC.

No daisy chaining of FMCM dump signals is required. If needed, this will be implemented outside the FMCM.

To give USER\_PERMIT = TRUE will require a minimum voltage/current of 2.8V at 12mA from the FMCM. CERN is responsible that specifications are met for all operational states and for all devices.

The protection grounds of the FMCM and the CIBU have to be connected for EMC reasons. The electronics ground of the FMCM and the protection ground are connected via a 1kOhm resistor. The ground in LHC will be good enough to guarantee a maximum voltage difference of 200mV between any two grounded points (changing magnetic fields are not expected, RF ground loops because of capacitance of protection diodes at CIBU input is not seen as a problem).

To protect the internal supply of the FMCM from short circuits in the connection cable (during e.g. commissioning and first connections) CERN recommends to insert a poly-switch protector in the +V line. Still, momentary power losses can occur in the FMCM



resulting in a data loss in the FMCM. This is accepted by CERN. The 'power up' time in minutes will be available in the status block to detect such power losses.

Additional resistors of 10 Ohms in the +V and -V line of the FMCM to the CIBU could further improve EMC behaviour and decrease the short circuit current in case of failure.

## 4. FUNCTIONAL REQUIREMENTS

### 4.1 HARDWARE

All power converters monitored by the FMCM are unipolar, only one FMCM device per electrical circuit is needed. The basic design of the FMCM will remain unchanged. As concerns the main system, adaptations of the box are required in order to comply with CERN standards.

#### 4.1.1 VOLTAGE DIVIDER AND ISOLATION AMPLIFIER

The measurement of the magnet voltage is done via connection to the power converter output terminals (in the transfer lines) or any other point in the electrical circuit (e.g. close to magnets in case of the LHC). A voltage divider and an isolation amplifier are installed for each measured voltage for galvanic isolation and adaptation of the signal before connection to the FMCM. The isolation amplifier is powered with  $\pm 20V$  from the FMCM and the maximum distance in between the FMCM and the amplifier is around 5m for the transfer lines and up to 100m for the LHC. Both, the design and installation of the isolation amplifier as well as the voltage divider are under the responsibility of the AB/PO group of CERN. The design of those two elements has to be radiation tolerant as in the LHC installation might have to take place close to the protected magnet(s).

#### 4.1.2 BACK PANEL



Figure 4: The current design of the FMCM back panel

The back panel will be adapted in the following way to satisfy the new requirements of CERN:

The currently individually placed 230 VAC connector, AC switch and protection fuse will be replaced by a line-filter of the type SCHAFFNER FN 282-2-06 (including fuse and interrupter).

- Remove the LEMO connectors for the Pre-Alarm (Dump+ Vorwarn), alarm output (Dump Out) and the optical alarm output (LWL Dump)
- Add the female Burndy 8 connector for the connection towards the BIC
- Add the female 9 pin D-Sub connector for the RS422 interface (Pins: 1=+RX, 2=-RX, 3=GND, 4=+TX, 5=-TX, 6..9=GND)
- The labeling of the front and back panel shall be changed to English labels

All other connectors remain on the back panel (HV-Box, U ext in, Digital I/O, DCCT in, Alarm Loop in -> now used for ext PM Trigger and Trig. I/O-> now used for UTC tick).

### 4.1.3 FRONT PANEL

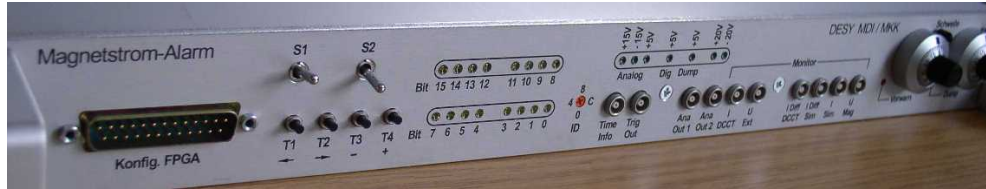


Figure 5: The current design of the FCMC front panel

The mechanics of the front panel remains basically unchanged. Two minor changes are to be implemented:

- The potentiometers for the thresholds of the alarm and the pre-alarm are safety critical and must not be easily accessible. They have to be either hidden by an enclosure or moved to the inside of the FCMC. Remote setting of the thresholds is not possible.
- Change to English labels

### 4.1.4 HARDWARE CHANGES OF THE PRINTED CIRCUIT BOARDS

#### 4.1.4.1 LOCAL POWER SUPPLY

The local power supply of the FCMC generates the required voltages for the analogue and digital electronics (+5V,  $\pm 15V$ ) as well as for the external isolation amplifier ( $\pm 20V$ ). The local supplies are all based on a transformer with single/double secondary winding(s), a rectifier bridge, a voltage regulator and a series of electrolytic capacitors for filtering of the output voltage. Although the supplies are not redundant, a reliability analysis showed an average failure rate of 1/12 years for all supplies of a FCMC, using very conservative values for the MTBF data of the used components. This is why the PCB for the local supplies will remain unchanged. If the FCMC's should contribute significantly to the number of false beam dumps during machine operation due to these local power supplies, a redundant design can be implemented rather easily in a later upgrade. In any case, a regular maintenance of the electrolytic capacitors (known to suffer from increased temperatures in the tunnel environment), is recommended e.g. every 5-10 years.

#### 4.1.4.2 MAIN PCB

To extend the functionality of the current design with the CERN requirements, the main PCB will be slightly changed with respect to the DESY version as follows:

- The dump pulse will be stretched by the FPGA (a maximum of 0.5 seconds will be foreseen; for first operation a pulse length of 50 ms will be used) to avoid multiple triggering during fast current ramps
- Keep the function of 'Pre-Alarms'. The pre-alarm threshold is normally set to  $0.5 \cdot \text{alarm level}$  and used for commissioning and the definition of 'good' alarm-thresholds. The pre-alarms are counted in the FPGA and available via the remote read-out
- Adapt the opto decoupled input to lower input voltages
- Change the transformer isolated input into an opto decoupled input to accept the UTC timing pulses

- Adapt design to improve EMC
- Replace capacitor pads with THT pads
- Insertion of buffer amplifiers into the monitor outputs (e.g. I\_SIM)
- Remove unused components on PCB, as e.g. the optical transmitter
- 2 I/Os of the FPGA used for RS-422 communication
- 2 I/Os of the FPGA used for the two user permit signals A & B (towards CIBU), using individual transistors for the two outputs
- Add 12 DIP-switches for the box identifier and hardware selection:
  - 6-bit identifier for the individual FMCM
  - 1-bit for selection of LHC or transfer line mode
  - 1-bit for selection of Alarm / no alarm functionality below 5% of the maximum voltage. In case the alarm functionality is selected, the FMCM will ALWAYS generate an alarm at its output if  $U_{mag} < 5\%$ . If deselected, the FMCM will NEVER generate an alarm if  $U_{mag} < 5\%$ . For  $U_{mag} > 5\%$ , functionality will only depend on the changes of the magnet current.
    - Value of the threshold is defined by a changeable resistor
  - 4 bits for future usage

## 4.2 FPGA PROGRAMMING

- Add alarm pulse stretching to a maximum of 0.5s to avoid multiple triggers for fast ramping magnets (especially in the transfer lines)
- Add serial byte receiver and transmitter (with parity) for control system interface
- Add state machine for control system interface
- Add function to individually activate the alarm outputs (see also chapter 6). The FPGA must never be able to simulate beam permit, but only to simulate beam dumps
- Change number, size, functionality and triggering of post mortem buffers:
  - Only the last event is visible in the Post Mortem Buffer instead of 8 buffers
  - 2000 values will be transmitted per channel, each value being a 12 bit analogue value
  - The 2000 values will either represent a time window of 30ms/-10ms with a resolution of 21.33 $\mu$ s or 60ms/-20ms with a resolution of 42.66 $\mu$ s
  - Implement the reception of the external Post Mortem Trigger
  - Post mortem trigger inhibit for a certain time after the last trigger to prevent overwrite of the buffer before reading (5 seconds for the transfer lines, 15 seconds for the LHC)
  - It is necessary that the VIP626 card can accept data blocks of 4096 Bytes at 115200 baud without data loss
- Adding the digital PLL for more accurate timing synchronization
- Add functionality of an alarm forcing/inhibit below 5% threshold
- Adding the status display functionality on front panel LEDs for a selected position of the HEX switch
  - Upper LED row: ON if TRUE

- **Bit 15:** Beam Permit A
- **Bit 14:** Beam Permit B
- **Bit 13:** Transmitting data via RS422 (TX)
- **Bit 12:** Receiving data via RS422 (RX)
- **Bit 11:** Always OFF
- **Bit 10:** Flash when UTC synch. Pulse received
- **Bit 9:** Flash when external PM trigger received
- **Bit 8:** Activate alarm below 5%
- Lower LED row:
  - **Bit 7:** LHC not TL mode
  - **Bit 6:** Always OFF
  - **Bit 5..0:** 6-bit ID

#### 4.2.1 FMCM TESTS AFTER FABRICATION

An EMC test of the FMCM is highly desirable and will be performed at CERN using the first batch of FMCMs to be delivered for May 2006. A qualification of the device to level 2 for industrial environments (ideally level 3 for highly perturbed industrial environments) of the norm is to be performed.

## 5. POST MORTEM

### 5.1 DATA STORAGE AND SIGNAL PROCESSING IN THE FMCM

The FMCM provides an internal 512k SRAM and an additional 32k NVRAM (able to keep data even in case of loss of the DC supply) for the storage of Post Mortem data. The ADC delivers 12-bit data of the measured signal, requiring thus 2 Bytes per stored value. A data set is decided to be 2000 values/signal. Signals that will be part of the PM data sent to the controls application are the following:

- Measured magnet voltage (12 Bit values)
- Simulated magnetic field changes (12 Bit values)
- DCCT current changes (12 Bit values, optional in the LHC, as distance to the converter might be very long)
- Interlock signal (1 Bit value, sent to the BIC via the CIBU interface)

The data structure and the content of each data word to be used for the post mortem data is defined as follows:

0000: First data word	(2 bytes)
.....	
3998: Last of the 2000 data words	(2 bytes)

Using:

Bit 11...0: analogue data word of selected channel

Bit 13...12: 0

Bit 14: opto isolated trigger (stretched to give at least one active sample), same for all channels (redundant)

Bit 15: FMCM alarm outputs (PERMIT A OR PERMIT B), same for all channels (redundant)

The measured (and simulated) values are continuously stored in the available memory. In case of an event, these buffers are frozen and the current signal data is stored. Two different versions of the PM buffer will be implemented. One for the transfer lines using the highest resolution of  $21.33\mu\text{s}$ , resulting in an available time window of -30ms before until +10ms after the event being available for the PM readout. Alternatively, for the slower LHC ramps this will be changed to a lower resolution (only every second value from the ADC is stored) and the time window increases to -60ms before until +20ms after the event.

A single buffer will be used for the storage of PM data, which is continuously overwritten with every new extraction. In case of transmission problems over the controls middle ware (CMW), data is stored locally and transmitted later in case of network problems.

In total, the transmission time of a PM Dataset is expected to be around 1.5 seconds at a transmission speed of 38400 Baud (115200 Baud will be used by the VIP626 card). This allows for resending of data in case of transmission errors without loss of data.

## 5.2 POST MORTEM TRIGGERS

In the transfer lines, an opto-isolated input will be used to connect the FMCM to the extraction pulse, received from the TG8 timing card installed in the ROCS-MUGEF crate of the power converter. An appropriate input circuit has been developed at DESY [7] and tested at CERN, using the TG8 and CTRP timing cards. The signal from the timing system is used for the freezing of the PM buffer. Multiple triggering during the ramp and the beginning of the flat top will already be suppressed by hardware (see chapter on hardware changes) and as such not create additional PM events.

In principle the PM data of all extraction events (even the ones where the FMCM did not react itself) can be transmitted to the control system. By default, the system will only request the transmission of PM data in case of faulty extraction events, while good extraction data could be transmitted on demand.

For the LHC there will be two independent trigger sources for each FMCM:

- Connection to the global PM trigger distributed via the CTRP card of the timing system (using the opto-isolated input)
- Self triggering of the device

In both cases, the trigger input receives in case of a PM event or Extraction a TTL pulse with a duration of  $\sim 2\mu\text{s}$  (continuously 5V, 0V for the trigger pulse).

In case of loss of the supply of the FMCM or continuous transmission problems over the network, PM data might be lost. Transmission of the PM data to the PM server is explained elsewhere (see also Appendix #2).

## 6. INTERFACING THE FMCM TO THE CERN CONTROL SYSTEM

The FMCM is connected via a serial RS422 interface to its VME front end computer and the CERN control system. This interface is exchanging data at 115200 Baud, using the following transmission protocol:

- Start bit + 8 bits of data + odd parity bit + 1 stop bit, full duplex

- Start each command with 10 \* <cr>
- If FMCM expects start of command and receives undefined byte, it answers with "?"
- Timeout if command to FMCM is not finished after 0.2 second (later option)

The command structure to be used is defined as follows (total of 20 Bytes):

00: 10 times <cr> for synchronization; <cr> = 0d(hex)

10: 1 byte <\*> to indicate start of command; <\*> = 2a(hex)

11: 1 byte command code (printing ASCII character lower case)

12: 6 bytes command argument

18: 2 bytes command checksum (sum of command code and command argument bytes referenced as unsigned chars + 55aa(hex), truncated to 16 bits)

Six different commands have been defined to command the FMCM via the RS422 interface:

- **t = Prepare** update of Timestamp:
  - Command arg (32 bit binary unsigned): 4 bytes binary indicating the UTC as Unix time stamp to be set at the next pulse at the time sync input; the remaining 2 bytes are not used.
  - Response: response header + 0 bytes data + response checksum + trailer = 32 bytes
- **d = Dump** (ch1 and / or ch2):
  - Command arg: first byte (ASCII): '1'= ch1 only, '2'= ch2 only, '3'= ch1 and ch2; then the following 5 bytes (to protect from accidental dump): "DUMP!" = 44, 55, 4d, 50, 21 (hex each)
  - Response: response header + 0 bytes data + response checksum + trailer = 32 bytes
- **s = Read Status**:
  - Command arg: "000000" (ASCII) = 30, 30, 30, 30, 30, 30 (hex each)
  - Response: response header + status data structure (see below) + response checksum + trailer = 64 bytes
- **p = Read Post Mortem Data** for selected channel (channels: Umag, Idiffsim, Idiffdct, Uext)
  - Command arg: first byte (ASCII): '0'=Umag, '1'=Uext, '2'=Idiffsim, '3'=Idiffdct; other 5 bytes: "00000" (ASCII) = 30, 30, 30, 30, 30 (hex each)
  - Response: response header + post mortem data structure (see below) + response checksum + trailer = 4032 bytes
- **r = Reset alarm counter** and / or pre-alarm counter
  - Command arg: first byte (ASCII): '1' (31 hex) = reset pre-alarm counter only, '2' (32 hex) = reset alarm counter only, '3' (33 hex) = reset pre-alarm and alarm counter + trailer = 32 bytes
  - Response: response header + 0 bytes data + response checksum
- **i = Idle command**: do nothing; can be used to check data transmission and „alive status“ by checking reflected command argument and timestamp in response header, or to stop the previous transmission
  - Command arg: any 6 bytes
  - Response: response header + 0 bytes data + response checksum + trailer = 32 bytes

The **response checksum** is defined as the sum of header bytes (starting from the initial <cr>) and all data bytes referenced as unsigned chars + 55aa(hex), truncated to 16 bits. **Trailer:** 2 bytes (**hex 3c 3e** = „<>“) signalling the end of the block

A **command example** in ASCII representation for the readout of post mortem data for the Uext could be as follows:

```
<cr><cr><cr><cr><cr><cr><cr><cr><cr><cr><cr> *p300000 <57(hex)> <3d(hex)>
```

The response header will be as follows (total of 28 Bytes):

00: 1 byte <cr> = 0d(hex)

01: 1 byte <\*> = 2a(hex)

02: 1 byte command code (copy from command received before)

03: 6 bytes command argument (copy from command received before)

09: 2 bytes checksum (copy from command received before)

11: 1 byte error bits:

Bit 0: Parity error

Bit 1: Framing error

Bit 2: Unknown command

Bit 3: Unexpected command argument

Bit 4: Checksum error

Bit 5: 0 (spare)

Bit 6: 0 (spare)

Bit 7: 0 (spare)

12: 7 bytes timestamp of NOW (4 bytes unsigned for integer second + 3 bytes unsigned integer for fractional seconds in  $2^{-24}$  seconds units: 1LSB = approx. 59.6ns)

19: 1 byte info bits

Bit 0: For mode LHC: last post mortem was triggered by ext. Trigger, not by alarm

Bit 1: Timestamp sync command came and next pulse on UTC input will update time

Bit 2: Timestamp initialized

Bit 3: Presently no reliable timestamp

Bit 4: Post Mortem Flag: inverted for every new post mortem dataset

Bit 5: Logic state of timestamp synchronization input (Input high = 1)

Bit 7...6: 0 (spare)

20: 7 bytes timestamp of last post mortem acquisition

27: 1 byte spare

The VME crate (housing the VIPC626 card for the connection of up to eight FCM systems via independent serial RS422 interfaces) is always the master of the data transmission. Priorities of data exchange and the according direction of data flow is always to be mastered by the front end. In normal operation, the FCM will send a continuous (short) message, including basic status data & settings. The status message is fixed to a total of 32 Bytes, whereas 31 Bytes of the message are already being filled by predefined data, leaving a single Byte spare. The transmission of this status message will require around 10ms. In case other data is judged to be more

important, data is to be removed out of the currently defined **status message structure** (total of 32 Bytes):

00: FPGA config. Version 1...255; 0=unknown	(1 byte)
01: Up-time in minutes (24 bits)	(3 bytes)
04: Pre-alarm threshold set by potentiometer	(2 bytes)
06: Alarm threshold set by potentiometer	(2 bytes)
08: Alarm counter (0...65535, stopped at max. value)	(2 bytes)
10: Pre-Alarm counter (0...65535, stopped at max. value)	(2 bytes)
12: Actual magnet voltage (1 sampled value, low accuracy is ok)	(2 bytes)
14: Actual voltage at connector Uext (=Uext, 1 sampled value)	(2 bytes)
16: Actual calculated field change (=Idiffsim, 1sampled value)	(2 bytes)
18: Actual DCCT current change (=Idiffdcct, 1sampled value)	(2 bytes)
20: Field deviation: min. of last minute	(2 bytes)
22: Field deviation: max. of last minute	(2 bytes)
24: New Timestamp minus FMCM timestamp at last time synchronization, signed integer, $1/2^{24}$ sec units, range $\pm 128$ seconds	(4 bytes)
28: ID and configuration status (Set by DIP switches, will not change during operation) (1 byte)	
Bit 5...0: Device ID (taken from DIP switch on add-on-PCB)	
Bit 6: Magnet type: LHC=1, TL=0	
Bit 7: =1 if Alarm activation below 5% demanded	
29: Device status (can change during operation)	(1 byte)
Bit 0: current alarm status channel A (0=USER_PERMIT=TRUE for CIBU)	
Bit 1: current alarm status channel B (0=USER_PERMIT=TRUE for CIBU)	
Bit 2: current status of opto-coupled input used for PM trigger (1=high)	
Bit 3: For mode „TL“: alarm was active during last extraction trigger (if YES: post mortem data should be read anyhow; if NO: data can be read optionally to compare with data of faulty magnets)	
Bit 4: 0 (spare)	
Bit 5: 0 (spare)	
Bit 6: 0 (spare)	
Bit 7: 0 (spare)	
30: 2 spare bytes	(2 bytes)

**Note:** The measurement of the all measured values (byte 12 of the status message) needs to be reformatted with a fixed gain and offset in the high level application.

The FMCM will be requested twice a second by the VME master to transmit this status message to the VME crate which is then forwarded to the supervision application and provided to the operator. The inclusion of the UTC time stamp and some measured voltages in this status message will indicate the operational state and communication of the FMCM to the operator.

Only upon a change of the timestamp of the 'Last Post Mortem acquisition' timestamp in the response header message (Byte 20...26), all other data transmission (such as



the status message or the timing message) will be temporarily suspended and the readout of the PM data will be requested by the VME.

The following priorities of data transmission are recommended (to be confirmed at the time of implementation):

- PM data
- Timing message (UTC time)
- Additional commands to the FMCM such as
  - Test the beam permit (inhibit) signals A & B (should be a safe transmission over CMW, e.g. hand-shake or double transmission of the request)
  - Reset of the alarm and pre-alarm counter (individual re-setting of the two)
  - Read-out command for transmission of the PM data
- Status message

For multi-byte values, big-endian coding will be used for their inclusion in the data structure and the following transmission (sending the most significant Byte first).

For a valid readout of one complete post mortem buffer, the VIP626 card has to be capable of receiving a block of at least 4096 Bytes at a the maximum transmission speed of 115200 Baud without any problems such as buffer overflows.

## 7. TIME STAMPING

For the time stamping of events, the FMCM will be synchronized to the UTC time, distributed by the timing system. The standard timing message will be received via the RS422 connection. This software message contains the UTC time as a 32 Bit value (absolute UNIX time in seconds since the 1<sup>st</sup> of January 1970). The device is synchronized upon reception of the next UTC tick to this previously received UTC time. For the FMCM, UTC synchronization should be done twice a minute.

For the reception of this UTC tick, the former transformer isolated input on the back panel of the FMCM will be used (to be transformed into an opto-decoupled input). In the transfer lines this input will be connected to a free output of the TG8 card in the ROCS. For LHC, an output of the CTRP card of the beam interlock controller will be configured for this purpose. A dedicated output will be provided to connect the FMCM clients to the TG8/CTRIP cards. If several FMCMs are to be connected, the use of a fan-out is possible (transparent to the user as the output stage is exactly the same as in the original timing card).

The TG8 card provides an open collector at its output (SN75471P with a 220 Ohm pull-up to 5V and a 1.8kOhm pull-down resistor), while the CTRIP card provides a driven output stage (74F3037). The TG8 provides a level of  $\sim 4.5V$  at its output (if terminated with high impedance), the CTRIP card delivers a peak-peak signal of  $\sim 3V$ .

For both cases, the FMCM will receive a TTL synchronization pulse with a duration of  $\sim 2\mu s$  (continuously 5V, 0V for the synchronization pulse) which is optimized for a 50 Ohm input. An appropriate input circuit for the reception of these timing signals has been developed at DESY [7] and tested at CERN, using the TG8 and CTRIP timing cards and 2m/60m of a coax cable similar to the RG58 type to test the correct reception of the timing pulses for the expected distances (see also Appendix #1).

The FMCM currently uses a quartz with an accuracy of 100ppm. The time base of the FMCM will be synchronized to the UTC time, received every 30 seconds. The UTC tick (corresponding to the previously received UTC message) is sent to the FMCM every

full second. The accuracy of the timing synchronization will be further improved via a digital PLL to be implemented in the FPGA program.

In order to increase the accuracy of the FMCM time stamp, an internal time base will be implemented with a resolution of  $\sim 100$ ns and a digital PLL loop will be implemented in the FPGA in order to guarantee continuous counting in case UTC ticks are missing and to avoid jumping of the counter.

In case of data transmission during a PM read-out, the counter value will be transmitted in 3 additional Bytes with the 4 Bytes UTC time via the RS422 interface to the high level application, allowing for time stamping of events with  $\sim 100$ ns.

## 8. MILESTONES AND PLANNING

First deadlines for an installation of the system will be the high intensity extraction tests in TI8 end of May 2006 and the following high intensity commissioning of the CNGS line. The LHC sector test will take place in December 2006 (no additional systems are required for this test). For end of May 2006 (high intensity extraction tests in TI8 and CNGS extraction tests), 10 FMCM monitors are required. They should already represent the final design of the FMCM for CERN. The remote-readout however can be implemented at a later stage.

Naturally, connections to the BIC and the power converter/electrical circuit have to be operational at this moment in time. If EMC tests are planned they should have been performed prior to these installations. Hardware for installation in TI2 and LHC will be required only at a later stage, depending when high intensity beam is foreseen in these installations.

## 9. REFERENCES

- [1] R.Schmidt: 'Fast Magnet Current Change Monitors', ECR, EDMS Doc.Nr:628602
- [2] V.Kain, '[Safe Injection into the LHC](#)' (Chamonix XIV)
- [3] B.Goddard et al: 'TT40 Damage during 2004 High Intensity SPS Extraction', AB-Note-2005-014
- [4] J.Wenninger et al.: 'Architecture of the SPS beam and extraction interlock systems', CERN-AB-2003-010-OP
- [5] M.Zerlauth: 'Magnet Powering System and Beam Dump Requests', Machine Protection Review, April 2005
- [6] M.Werner (DESY): 'Magnetstrom-Alarme für HERA', HERA Seminar, Grömitz
- [7] M.Werner (DESY): Input circuit for connection of the FMCM to the CERN timing cards, private communication

## 10. APPENDIX #1

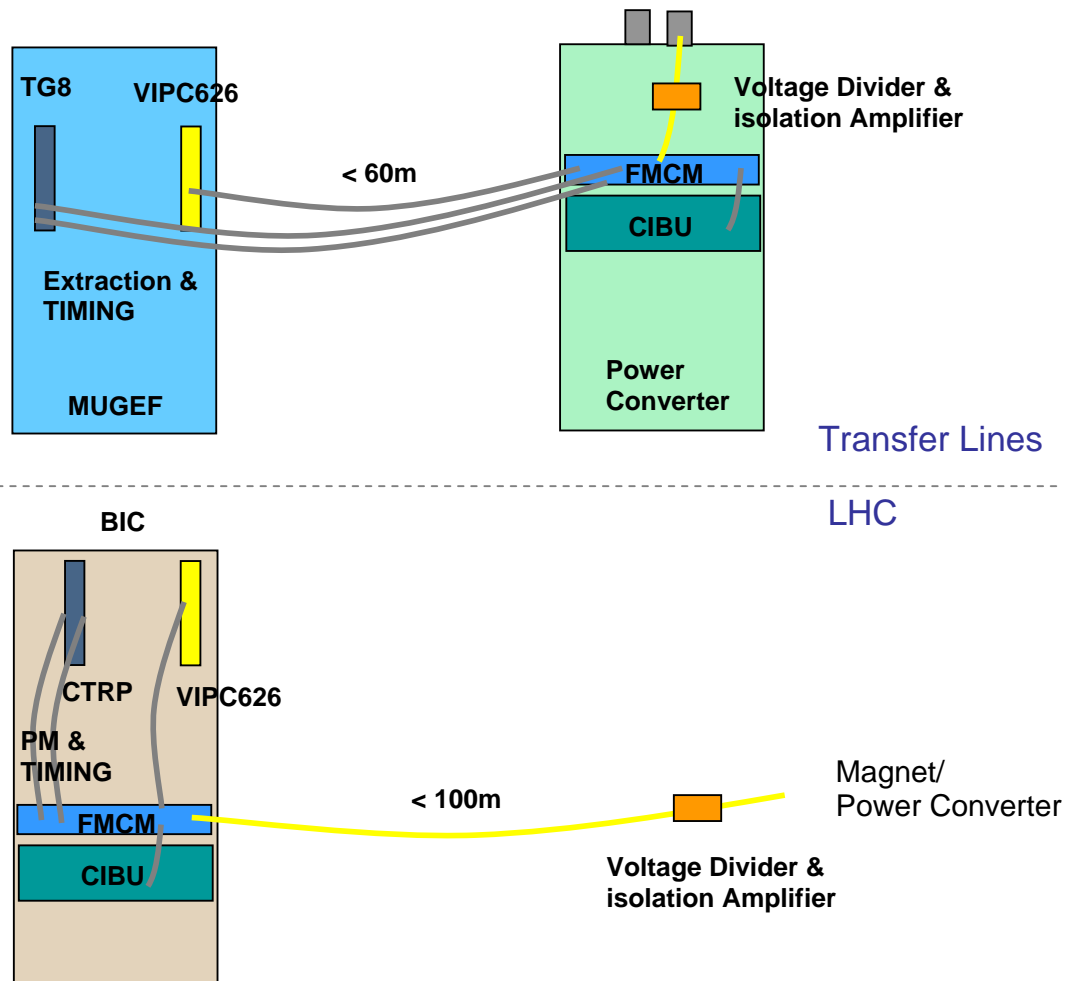


Figure 6: Distribution of system components in the transfer lines and LHC installations

## 11. APPENDIX #2

Once the PM data has been received via the RS422 interface in the VME front end (the ROCS-MUGEF in case of the transfer lines and the BIC in case of the LHC), the PM data is to be sent in a binary format via CMW to the PM server.

Additional meta information (such as system id, device class, device id, event timestamp etc.) will be added as separate fields in the CMW structure at the front end level. A typical CMW structure as used by the power converter group during a dry run test could like as follows:

```
<?xml version="1.0" encoding="windows-1252" ?>
- <binx>
- <definitions>
- <defineType typeName="po_header_struct">
- <struct>
  <unsignedInteger-32 varName="sequence" />
```

```

    <integer-32 varName="time_sec" />
    <integer-32 varName="time_usec" />
  </struct>
</defineType>
- <defineType typeName="po_record_struct">
- <struct>
  <unsignedByte-8 varName="status" />
  <unsignedByte-8 varName="class_id" />
  <unsignedByte-8 varName="interlocks" />
  <unsignedByte-8 varName="faults" />
  <unsignedByte-8 varName="warnings" />
  <unsignedByte-8 varName="measurements" />
  <unsignedByte-8 varName="pll_op_states" />
  <unsignedByte-8 varName="vs_pc_states" />
  <float-32 varName="imeas0" />
  <float-32 varName="imeas1" />
  <float-32 varName="iref" />
  <float-32 varName="vref" />
</struct>
</defineType>
</definitions>
- <dataset src="pmdata.bin" byteOrder="bigEndian">
- <arrayFixed varName="PO_data">
  <dim indexTo="2999" />
- <struct>
  <useType typeName="po_header_struct" varName="header" />
- <arrayFixed>
  <dim indexTo="29" />
  <useType typeName="po_record_struct" />
</arrayFixed>
</struct>
</arrayFixed>
</dataset>
</binx>

```

The interface in between the client and the PM server is still under discussions, but it is very likely that a dedicated client API will be provided to have a generic transmission of PM data to the server.

The data structure of the binary data from the FMCM can be arranged in e.g. 4 arrays of different types (one for each PM signal), or a single array of structures that contain several fields of different types.

The length of each data set from the FMCM is fixed to 2000 values. Upon reception of data, the PM server receives the data as it comes in a binary file. An independent process converts that binary to an ASCII format (probably SDDS).

## 12. APPENDIX #3

FCCM Nr	Converter name	Used in the Transfer Line / LHC Insertion	Circuit is ramped using cycle Type	di/dt max [A/s]	Inom max [A]	I max DCCT [A]	I max Conv.	Precision (+/-) of I max	Load R mΩ	Load L mH	U max Conv.	Detection Level (+/-) of I max	Detection Time ms	Temperature effect on flat top Adiabatic calculation! K/s
1	MST 6177M	TT60	TI2 ~ TI8		7200	7500	7500	1*10 <sup>-4</sup>	3.21	0.039	59	5*10 <sup>-3</sup>	0.1	8.587
2	MSE 6183M	TT60	TI2 ~ TI8		22000	24000	24000	1*10 <sup>-4</sup>	3.59	0.083	80	5*10 <sup>-3</sup>	0.1	14.605
3	MBB 2015M	TI2	TI2 ~ TI8		3690	4400	4400	5*10 <sup>-5</sup>	16	20	160	3*10 <sup>-3</sup>	2.7	0.322
4	MBI 2213M	TI2	TI2 ~ TI8		5150	5400	5400	5*10 <sup>-5</sup>	290	224	1800	3*10 <sup>-3</sup>	2.7	0.184
5	MBIBH 2931M	TI2	TI2 ~ TI8		725	800	810	5*10 <sup>-5</sup>	477	618	450	3*10 <sup>-3</sup>	7.9	0.114
6	MSIB 2952M	TI2	TI2 ~ TI8		950	1000	1620	1*10 <sup>-4</sup>	107	124.6	210	3.5*10 <sup>-3</sup>	3.5	0.149
7	MSE	TT40	CNGS & TI8		22000	24000	24000	1*10 <sup>-4</sup>	3.59	0.083	80	2*10 <sup>-3</sup>	0.1	14.605
8	MBHC 4001M	TT40	CNGS & TI8		900	1000	1000	1*10 <sup>-4</sup>	225	227.4	300	5*10 <sup>-3</sup>	5.1	0.573
9	MBHA 4003M	TT40	CNGS & TI8		1000	1100	1000	1*10 <sup>-4</sup>	184	480	550	1*10 <sup>-3</sup>	5.0	0.073
10	MBI 8160M*	TI8	TI8		5250	5400	5400	5*10 <sup>-5</sup>	528	472	3600	3*10 <sup>-3</sup>	2.7	0.191
11	MBIAH 8783M	TI8	TI8		900	1000	1000	1*10 <sup>-4</sup>	319	840	600	3*10 <sup>-3</sup>	7.9	0.059
12	MSIB 8813M	TI8	TI8		950	1000	1620	1*10 <sup>-4</sup>	102	124.6	210	3.5*10 <sup>-3</sup>	3.5	0.149
13	MBSG 4100M	TI8 / CNGS	CNGS & TI8		3810	4400	6000	1*10 <sup>-4</sup>	57	60	510	1*10 <sup>-3</sup>	4.0	0.458
14	MBG 4101M*	CNGS	CNGS MBG		5100	5400	5400	5*10 <sup>-5</sup>	402	416.1	3600	6*10 <sup>-4</sup>	4.0	0.339
15	RD1.LR1	IR1	LHC	2.02	810	1000	810	1*10 <sup>-4</sup>	854	1740	950	3.5*10 <sup>-4</sup>	0.9	
16	RD1.LR5	IR5	LHC	2.02	810	1000	810	1*10 <sup>-4</sup>	849	1740	950	3.5*10 <sup>-4</sup>	0.9	
17	RMSD.LR6B1	IR6	LHC	8.25	880	1000	1000	1*10 <sup>-4</sup>	529	855	600	5*10 <sup>-4</sup>	1.0	
18	RMSD.LR6B2	IR6	LHC	8.25	880	1000	1000	1*10 <sup>-4</sup>	529	855	600	5*10 <sup>-4</sup>	1.0	
19	RD34.LR3	IR3	LHC	2.25	720	1000	810	1*10 <sup>-4</sup>		2160	950	> 3.5*10 <sup>-4</sup>	> 1.0	
20	RD34.LR7	IR7	LHC	2.25	720	1000	810	1*10 <sup>-4</sup>		1440	950	> 3.5*10 <sup>-4</sup>	> 1.0	

Table 3: Detailed circuit parameters for FCCM installations