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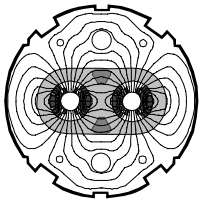

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Engineering Specification

THE HARDWARE INTERFACES BETWEEN POWERING INTERLOCK SYSTEM, POWER CONVERTERS AND QUENCH PROTECTION SYSTEM

Abstract

The Machine Interlock System includes Powering Interlocks and Beam Interlocks to protect the equipment of the LHC [1]. The Powering Interlock System is designed to ensure the permission for powering the different electrical circuits with superconducting magnets installed around the accelerator. It protects equipment in case of magnet quench or failure of other components (power converters, magnet protections, switches for energy extraction) and takes the appropriate action to minimise recovery following a powering abort.
This specification defines the hardware interfaces of the interlock system with the power converters and the quench protection system.

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History of Changes

Rev. No.	*Date*	*Pages*	*Description of Changes*
0.1	14/8/2002		Comments from Markus and Bruno included
0.2	10/9/2002		Comments from Valerie included
0.3	22/10/2002	20	QPS_DISCHARGE renamed into CIRCUIT_DISCHARGE
0.4	20/12/2002	several pages	Interface for MQM magnets included, additional drawings for interface between interlocks and RB circuit in odd points. Additional drawings for interface PIC-QPS in odd points for RB circuits. Tables updated
	17/01/2003	All	Submission for engineering check
	22/04/2003		Circuits RD1, RD2, RD3 and RD4 do not need heater firing and change classification
			Clarification of subclasses for hardware interfaces, and consistent renaming of cables
			Including the comments of Bruno, Valerie, Reiner and Markus
			Replacement of the concept of “circuit classes” by two variables for each circuit.
0.5	20/06/2003	All	Submission for check
0.6	24/04/2004	All	Including comments of Valerie and Reiner after engineering check, update to layout version 6.402
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1.0	01/09/2004	All	Including comments of Valerie, Felix and Karl-Hubert after engineering check • TOTEM suppression • Adding EE system in Figure 5 • Change of circuit class from B2->B1 for RD circuits • Renaming of circuits RSRU->RU • Revision of signal naming (see Appendix E)
2.0	07/09/2004	All	Released Version
	14/02/2005		Page 17: Change the notation ‘8 female poles’ to ‘8 male poles’
			Page 18: Change the notation ‘12 female poles’ to ‘12 male poles’
2.1	17/04/2007	All	Update of interlock drawings in Appendix C
			Delete obsolete Appendix E on signal naming. Align signal names and current loop names and make reference to Naming DB
			Additional drawing for interface PIC/QPS for RB/RQD and RQF circuits in new Appendix E
			Update of distribution list
	19/04/2007	All	Submission for engineering check
			Including comments of Bruno, Stephen, Rudiger, Valerie and Ronny, adding paragraph on 60A power permit signal distribution (section 6.4)
2.2	21/06/2007	All	Submission for approval
3.0	23/08/2007	All	Released version

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1. INTRODUCTION

The architecture of the Machine Protection System has been described in “Machine Protection for the LHC: Architecture of the Beam and Powering Interlock Systems” [1].
Two interlock systems have been proposed, for beam operation to be ready for the LHC start-up with first injection of beam and for the powering system already required for hardware commissioning of LHC powering subsectors.
In [2] the powering subsectors were defined. For each powering subsector, a powering interlock controller (PIC) handles the interlocks (two PICs for the long arc cryostats).
This specification describes the hardware links of the powering interlocks with the quench protection system (QPS) and the power converter system (PC). It is based on the LHC Layout version 6.501.

2. PURPOSE

- Definition of the functionality of the Powering Interlock System and the signal exchange with power converters and the quench protection system.
- Assignment of each electrical circuit to a specific “hardware interface type” that determines the interfaces between powering interlock controllers, power converters, quench protection and energy extraction system.
- Definition of the types of cables between powering interlock controllers, power converters and quench protection system for each hardware interface type, including the detailed pin assignment.
- Assignment of two variables to each electrical circuit that determine the response in case of a failure in one electrical circuit with respect to other electrical circuits in a subsector, and to beam operation.

3. FUNCTIONALITY OF THE POWERING INTERLOCK CONTROLLER: GENERAL ASPECTS

In case of a quench or another failure during powering of LHC magnets, the magnetic energy has to be extracted as fast as possible. The time constant for the current decay can be large. For example, the time constant for the discharge of the main dipole magnets is 100 s. The number of superconducting magnets in the LHC exceeds 10000, with about 2000 large dipole and quadrupole magnets, and 8000 corrector magnets. The superconducting magnets are powered in 1618 electrical circuits, with nominal currents of 12 kA, 4-8 kA, 600 A, 120 A and 60 A. Conduction and gas cooled copper current leads are used to power the 120 A and 60 A orbit corrector circuits. The current leads with higher current capacity (including the 120 A spool-piece octupole circuits) use high temperature superconducting (HTS) material.

4. SIGNALS BETWEEN THE POWERING INTERLOCK SYSTEM, POWER CONVERTERS AND QUENCH PROTECTION SYSTEM

The powering system includes electrical circuits with 154 dipole magnets operating at a current of up to 12 kA and a stored energy in the magnets of one circuit of 1.2 GJ. It also includes circuits with single corrector magnets operating at a maximum current of 60 A and stored energy of only several kJ. Many other circuits have parameters in between these two extreme cases. Consequently, the interfaces between power converters, quench protection and interlock system depend on the type of electrical circuit.

- For all circuits, except for the 60A orbit corrector circuits that are not connected to the powering interlock system, a signal “green light” for powering is issued by the

PIC that permits the power converter to start, called CMD_PWR_PERM_PIC. If the signal is not present, the power converter performs a slow power abort and goes OFF.

- In case of an internal failure detected by the power converter, a signal POWERING_ FAILURE is issued. Such failures include failures of the power converter itself, failures in the supply (water, electricity), etc.
- For an emergency stop of the power converter, for example after a quench, the power converter receives the signal PC_FAST_ABORT. For some of the circuits (600 A) with large stored energies an additional energy extraction system is installed in a rack beside or behind the power converter. The energy extraction system will receive the signals ST_FPA via the same current loop.
- For all circuits with quench detectors the quench protection system issues a signal in case of quench: ST_CIRCUIT_OK_QPS.
- For some circuits, the power converter requests a discharge of the energy, if a failure in the water-cooling of the free-wheel path is detected (as the free-wheel path would not survive a long current decay time without cooling). For such cases, the power converter issues the signal PC_DISCH_RQ. The energy extraction system for some of the circuits is part of the quench protection system. In order to initialise energy extraction, the signal ST_CMD_DISCHARGE_QPS is received by the quench protection system.

5. DEFINITION OF THE HARDWARE INTERFACES

The exchange of hardware signals must be fail-safe. High reliability is required after a detection of the quench by a quench detector, when the power converter of the corresponding circuit needs to receive a fast power abort. High reliability is also required in case of a request from the power converter for energy extraction, when the QPS must trigger the discharge of energy in the associated circuit.
Some requirements for the interfaces:

- The interfaces should be reliable
- The interfaces should be simple
- The cost of the implementation should be considered

When addressing reliability, the following failures were considered:

- Failure of the powering interlock controller
- Failure that a relay does not open when requested
- Failure of the power converter that does not switch off
- Failure of a bad connection (for example, cable not plugged into one system, broken wire or pin)
- Failure with a short circuit between to wires within a connector, or in a cable

The considerations to design a fail safe system led to the block diagrams of the current loops shown in Figure 4 to Figure 12 with the signals defined in Table 1. Up to four current loops linking all systems involved will be used to exchange the required protection signals for an electrical circuit. By definition, the system requesting a signal provides the current in the loop. The loops will be driven by a **voltage between 15 V and 24 V**. The **loop current** should be **between 10 mA and 20 mA**. The maximum allowed voltage drop of each system in the current loop is 2.5 V.

The *Powering Permit Loop* and the *Powering Failure Loop* represent a one-to-one connection between power converter and PIC. For these two interfaces, loops shown in Figure 4 and Figure 5 (Figure 7 and Figure 8 for MQM/MQY) are transmitting the

according protection signals (which will have different names depending on the system issuing or receiving the signal – see also Table 1).

The *Circuit Quench Loop* and the *Discharge Loop* connect all three systems to take appropriate actions in all systems in case of quench or a discharge request by the power converter or the PIC.

Any failure of the PIC, for example wrong programming or faulty data, would possibly result in a fast power abort of the converter but not in damage of equipment.

Loop name	*Name of the signals concerned*	*Signal direction*	*Description*
Powering Permit LOOP	CMD_PWR_PERM_PIC	Issued by PIC	Issued by PIC if all conditions for safe powering are met
	PC_PERMIT	Received by PC	Power Permit signal received by PC
Powering Failure LOOP	ST_FAILURE_PIC	Received by PIC	Powering Failure signal received by PIC
	POWERING_FAILURE	Issued by PC	Issued by PC in case of internal failures
Circuit Quench LOOP	PC_FAST_ABORT	Received by PC	Fast power abort received by PC after e.g. quench detected by QPS, or after fast power abort request from PIC
	ST_CIRCUIT_OK_QPS	Issued by QPS	Quench signal issued by QPS for this circuit (in case of quench signal becomes FALSE)
	CMD_ABORT_PIC	Issued by PIC	Fast Power Abort issued by the PIC (after e.g. a global powering subsector abort)
	ST_ABORT_PIC	Received by PIC	Quench signal received by the PIC
	ST_FPA	Received by EE	Fast Abort request received by the energy extraction system
	ST_SUM_FAULT	Issued by EE	Fast Power Abort issued by EE due to internal fault
Discharge LOOP	ST_CMD_DISCHARGE_QPS	Received by QPS	Energy discharge request received by QPS after demand from PC or PIC
	ST_DISCHARGE_PIC	Received by PIC	Energy discharge request received by PIC
	CMD_DISCHARGE_PIC	Issued by PIC	Energy discharge request issued by PIC
	PC_DISCH_RQ	Issued by PC	Energy discharge request issued by PC

Table 1: Hardwired current loops and signal names of signals between PIC, QPS and PC

Note! The complete set of signal names along with an according description can be found in the Naming DB of the AB/CO/DM section [3]. Signal names for power converters in this specification refer to the hardware level and do not match the names of software properties manifested by the FGCs and visible via the control system (see Appendix H for correlation table).

In addition, high reliability for the following four operations is required:

1. Opening of the *Circuit Quench LOOP* by the QPS after a quench
2. Opening of the *Discharge LOOP* by the power converter after a failure in the water cooling
3. Reception of a discharge request and triggering a discharge by the QPS
4. Reception of a fast power abort, and triggering the fast abort procedure by the power converter

How to fulfil these requirements is left to the system designers and is not discussed here.

One risk is a short circuit between two wires. In this case, signals in the loop would not be transmitted correctly. To minimise such failure it is suggested:

- Testing the signal transmission after every intervention. With the quench protection system in test mode, it will be possible to open one of the relays in the quench detector and observe if the fast power abort signal arrives at the PIC and the power converter. The PIC and the power converters should provide similar test features.
- When the system is left running without intervention and without touching the cables, it is very unlikely that such failure would occur.

For the interfaces, multi-wire cables will be used (defined in the appendix). Two wires in the cables will be used for the PIC to verify the connection of a cable between PIC and power converter, or PIC and QPS:

- PC_CONNECT
- QPS_CONNECT

This requires a bridge between two pins of the connector on the PC / QPS side (for the definition see appendix).

6. HARDWARE INTERFACE TYPES

Since the interfaces depend on the type of electrical circuit, several **hardware interface types** are defined. Each electrical circuit is attributed to one hardware interface type (see Table 2 for details). Some electrical circuits have more than one power converter (segmented circuits), for example the inner triplets circuits with MQXA/B magnets in point 1,2,5 and 8 (see interface type A), and circuits with MQM/MQY magnets (see interface type B2). In case of a quench, one quench signal is received by the PIC. One CMD_ABORT_PIC is issued for all power converters in the circuit that are then switched off.

	Hardware Loops between PIC and PC						HW Loops between PIC and QPS		
Hardware Interface Type	PC Connect	Powering Failure	Discharge	Powering Permit I	Powering Permit II	Circuit Quench	QPS Connect	Circuit Quench	Discharge
A1	YES	YES	YES	YES	NO	YES	YES	YES	YES
A2	NO	NO	NO	NO	NO	NO	YES	YES	YES
B1	YES	YES	NO	YES	NO	YES	YES	YES	NO
B2	YES	YES	NO	YES	YES	YES	YES	YES	NO
C	YES	YES	NO	YES	NO	NO	NO	NO	NO
(D)	(NO)	(NO)	(NO)	(NO)	(NO)	(NO)	(NO)	(NO)	(NO)

Table 2: Hardware Loops and Interface Types

6.1 HARDWARE INTERFACE TYPE A

Such interface is required for 32 circuits (see Table 3 and Table 4 in Appendix D). Electrical circuits with an interface type A store in general a large amount of energy. In case of a quench, the switch of the energy extraction system is directly opened by the QPS. Energy extraction in case of a failure of the cooling system of the power converters is required since the time constant for discharge is long. The power converter requests the discharge of energy and the QPS initiates energy extraction in the following way:

- If a system for energy extraction is present, the QPS opens the energy extraction switch (for RB, RQF and RQD)
- If there is no discharge resistor in the circuit, the QPS fires the quench heaters on all the magnets in the circuit (RQX)

Interface type A1 determines the interface of the PIC to the PC and the QPS at the even points. For the connection of the PIC with the QPS for the energy extraction system of the dipoles (odd points) interface type A2 is applied.

Main dipole circuits: the power converters for the main dipole circuits are always located in underground areas close to the even points. The energy in the magnets is extracted with one extraction system close to the even point, and a second extraction system close to the odd point. There is one cable per circuit between PIC and QPS and PIC and power converter at the even points, and one cable between the PIC and QPS at the odd points that allows the PIC to trigger extraction of the energy and to receive the circuit quench signal (see Figure 17 for details).

MQX Triplet: Powering of the main inner triplet magnets is shown in Figure 1. If one of the magnets quenches, all heaters are fired, and all power converters in the circuit perform a fast power abort. There is one cable between the PIC and the QPS for the quadrupole magnets in the triplet, and one cable from the PIC to the set of three power converters (connected in series) supplying the current to the magnets.

Main quadrupole circuits: The focusing and defocusing main arc quadrupole circuits are connected with interfaces of type A1. There is one power converter in the circuit, one cable per circuit between PIC and QPS, and one cable between PIC and power converter.

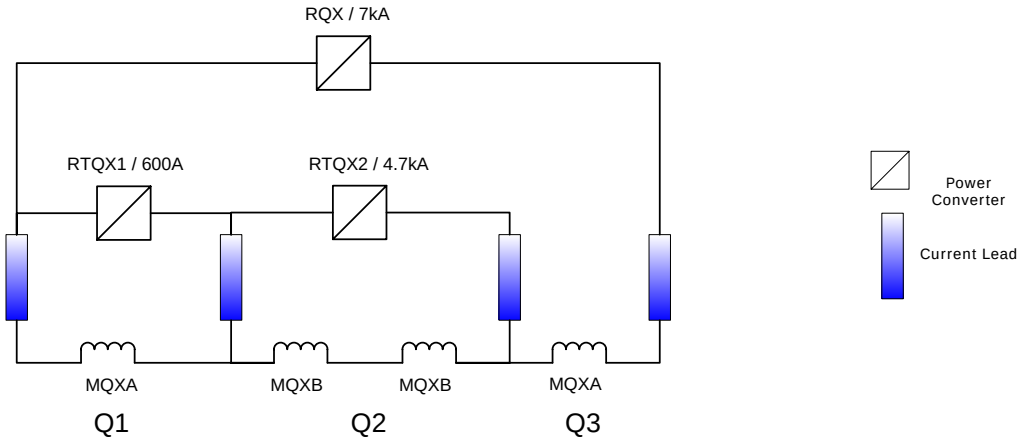

Figure 1: Electrical circuit configuration for inner triplets in IR1, IR2, IR5 and IR8

6.2 HARDWARE INTERFACE TYPE B

This interface is required for about 514 circuits (see Table 3 and Table 4 in Appendix D). The power converter does not need to request the fast discharge of the energy, as the time constant for the decay of the current is short. When a magnet quenches, the quench heaters are fired and the QPS notifies of the occurred quench by removing the signal ST_CIRCUIT_OK_QPS. Some of the circuits require extraction of the energy in case of a quench. The energy extraction is activated when the power converter receives the ST_FAULTS:FAST_ABORT signal since it is connected to the same current loop.

There will be one cable between the PIC and the QPS that includes the signals ST_CIRCUIT_OK_QPS for up to four circuits.

Interface type B2 describes the interface of the PIC to the power converters and the QPS for all the MQM/MQY circuits, while type B1 is used for all other remaining circuits of interface type B.

MQM/MQY magnets: Powering of the magnets is shown in Figure 2. If one of the two magnets quenches, all heaters are fired, and both power converters in the circuit perform a fast power abort. There is one cable between the PIC and the QPS for both quadrupole magnets, and one cable from the PIC to the two power converters supplying current to the quadrupole magnets. There will be one ST_CIRCUIT_OK_QPS signal from the QPS system to the PIC. The PIC handles the two power converters as a single circuit, except for the CMD_PWR_PERM_PIC signal that is supplied to each power converter (see Appendix C for Interface drawings) and which will be called CMD_PWR_PERM_B1_PIC and CMD_PWR_PERM_B2_PIC. If one of the converters fails, the other is switched off simultaneously by the PIC.

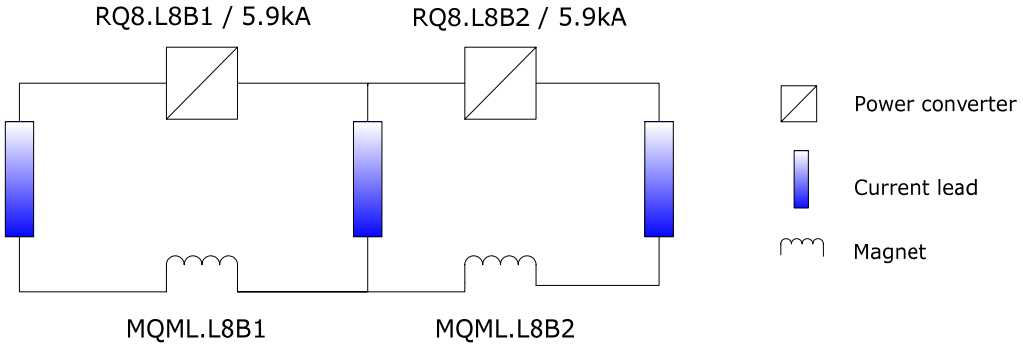

Figure 2: Circuit diagram for individually powered quadrupoles (MQM/MQY) in the LSS and the DS Regions (using the example of the circuit RQ8.L8, powering the magnets MQML.L8B1 and MQML.L8B2)

6.3 HARDWARE INTERFACE TYPE C

This interface is required for about 274 circuits (see Table 3 and Table 4 in Appendix D). There is no quench detection system for the elements in the circuits, and therefore no cable between QPS and PIC. The PIC manages the CMD_PWR_PERM_PIC, and receives the ST_FAILURE_PIC to possibly request a beam dump. In general, circuits with interface type C are for magnets with little stored energy.

For this interlock type (electrical circuits operating at a maximum current of 80 A and 120 A), the power converters are grouped in a rack with up to four 4 converters. One cable between PIC and one rack is installed. For each circuit, the signals CMD_PWR_PERM_PIC and ST_FAILURE_PIC are exchanged. In addition, there is one signal PC_CONNECT per cable to indicate if the cable between the PIC and the rack is connected.

6.4 HARDWARE INTERFACE TYPE D

This interface type includes all 752 orbit corrector magnets powered with converters installed under the main magnets of the arc cryostat at a maximum current of 60 A (see Table 3 and Table 4 in Appendix D). No hardware link exists between the PIC and the elements of this circuit type, but a global power permit signal is transmitted via the controls and timing system to all converters in each of the eight sectors when all conditions for powering in the long arc cryostat are met.

For each sector one common PC_PERMIT_60A signal is generated by the SCADA system of the powering interlock system (derived from a collection of cryogenic and powering conditions in the related powering subsector) and sent via CMW to the timing system, which in turn will include these 8 Bits into the telegram group PP60A (with the according Payload of 8 Bits, called : 'Arc12', 'Arc23', 'Arc34', 'Arc45', 'Arc56', 'Arc67', 'Arc78', 'Arc81') as shown in Figure 3 and the timing event HX.PP60A-CT.

The calculation for the example of the arc cryostat in sector 78 is the following:

ST_CRYO_MAINTAIN & "COM_CIP-CFP_PVSS_STATUS" & "COM_CRYO-CFP_CIP-CFP_STATUS" for CIP.TZ76.AR7 &
ST_CRYO_MAINTAIN & "COM_CIP-CFP_PVSS_STATUS" & "COM_CRYO-CFP_CIP-CFP_STATUS" for CIP.UA83.AL8

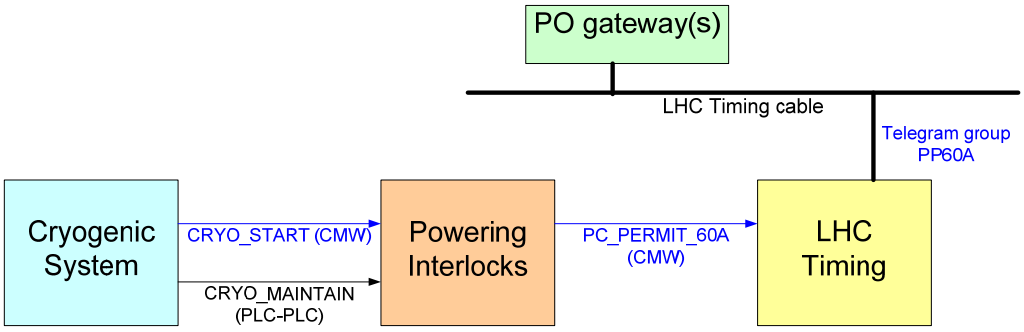

Figure 3: Distribution of power permit signal for 60A converters

The LHC telegram is sent once a second over the timing cable and used by the PO gateways (which will distribute the information to the connected FGCs) upon start-up to initialise the state of the signal. The signal has the same functionality as the PC_PERMIT for the other circuit types and will result in a slow power abort of the power converter upon removal. After start-up, further updates are received in the form of the HX.PP60A-CT timing event, giving a response time far better than the 1 second update of the telegram.

Note: Loss of communication between any of the systems will not result in a power abort (with the exception of communication loss between the interlock SCADA system and its front-ends), but the last valid data received will be kept (and continued to be distributed) in order to allow for re-boots of e.g. gateways without aborting powering of these converters. In case the FGC receives no packets from the gateway for (600 +2*FIP_ID) seconds, an automatic slow power abort will be initiated. This is acceptable as this link is implemented to improve operational efficiency, as protection of the superconducting elements is always guaranteed by the connected power converter.

7. INTERLOCK VARIABLES FOR ELECTRICAL CIRCUITS

For each circuit, two variables are introduced defining specific actions taken by the PIC software in case of a failure.

After a quench in a magnet or a failure in the powering system for this circuit, the PIC receives a signal (ST_CIRCUIT_OK_QPS or ST_FAILURE_PIC). The PIC needs to take two decisions:

- POWERING SUBSECTOR OFF

  Is it required to abort powering in the subsector, and to extract the energy as fast as possible? The decision depends on the energy released by the magnet that quenched. If the quench could propagate to other magnets, powering should be aborted. If the energy is small, there is no reason to abort powering.

- ESSENTIAL FOR BEAM

  Is it required to dump the beam? If the magnets in a circuit are essential for operation with beam, the beam should be dumped. A circuit is defined to be essential for beam operation if no particles can circulate without the magnets in the circuit.

The variables of electrical circuits are used by the PIC and have no impact on the hardware interfaces. The process in the PIC depends on both, the hardware interface type and the values of the variables (see also Appendix E for details).

8. CONCLUSIONS

The powering interlock system is required for the hardware commissioning of the first LHC sector.

The detailed functionality of the powering interlock controller will be described in a future specification.

This specification does not include the interfaces between power converters and machine interlock system for the protection system of normal conducting magnets, which is defined elsewhere [5].

Modifications of the attribution of an electrical circuit to a hardware interface would lead to changes of the cables and connectors, and should be avoided.

Modifications of the value of the variables of an electrical circuit in the LHC Functional Layout Database will be possible at any time without modifying hardware, but will require a reconfiguration and downloaded of the new parameters into the corresponding PICs. However, such modifications should be carefully implemented and commissioned, as a change of these parameters might introduce additional stress and risk for the equipment.

9. ACKNOWLEDGEMENT

The basic ideas were developed in a close collaboration between F.Bordry, R.Denz, K.H.Mess, F.Rodriguez-Mateos, together with the authors. We also like to thank numerous other colleagues that have been involved in the discussions.

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Appendix A: Cables between PIC and PC

Hardware Interface Type A1 – Cable ID: A1-PIC-PC

A 10-wire cable (NE10) has been chosen for the interface between power converter(s) and PIC for each circuit. The type of the connector at each end of the cable is a 12 male poles Burndy connector, type 12BPMB with the following pin assignment:

Name	PC side or PIC side	NE 10 Wire
POWERING FAILURE LOOP +	Pin 1	1
POWERING FAILURE LOOP -	Pin 2	2
DISCHARGE LOOP +	Pin 3	3
DISCHARGE LOOP -	Pin 4	4
PC_CONNECT +	Pin 5	5
PC_CONNECT -	Pin 6	6
CIRCUIT QUENCH LOOP +	Pin 7	7
CIRCUIT QUENCH LOOP -	Pin 8	8
Spare	Pin 9	n.c.
Spare	Pin 10	n.c.
POWERING PERMIT LOOP +	Pin 11	9
POWERING PERMIT LOOP –	Pin 12	10

Hardware Interface Type B1 – Cable ID: B1-PIC-PC

A 10-wire cable (NE10) has been also chosen for the interface between power converter(s) and PIC for each circuit. The type of the connector mounted on the cable at the end of the power converter is a 12 male poles Burndy connector (type 12BPMB), and an 8 male poles Burndy connector (type 8 BPMB) at the PIC side, with the following pin assignment:

Name	PC side	PIC side	NE 10 Wire
POWERING FAILURE LOOP +	Pin 1	Pin 1	1
POWERING FAILURE LOOP -	Pin 2	Pin 2	2
Spare	Pin 3		3
Spare	Pin 4		4
PC_CONNECT +	Pin 5	Pin 3	5
PC_CONNECT -	Pin 6	Pin 4	6
CIRCUIT QUENCH LOOP +	Pin 7	Pin 5	7
CIRCUIT QUENCH LOOP -	Pin 8	Pin 6	8
Spare	Pin 9		n.c.
Spare	Pin 10		n.c.
POWERING PERMIT LOOP +	Pin 11	Pin 7	9
POWERING PERMIT LOOP –	Pin 12	Pin 8	10

Ground connection: it is required to always connect both sides of the cable shielding (“tresse”) to minimise possible electromagnetic interference.

Hardware Interface Type B2 – Cable ID: B2-PIC-PC

A 10-wire cable (NE10) has been chosen for the interface between power converter(s) and PIC for each circuit. This hardware interface type is valid for circuits with MQM, MQMC, MQML and MQY magnets. The type of the connector at each end of the cable is a 12 male poles Burndy connector, type 12BPMB with the following pin assignment:

Name	PC side or PIC side	NE 10 Wire
POWERING FAILURE LOOP +	Pin 1	1
POWERING FAILURE LOOP -	Pin 2	2
Spare	Pin 3	n.c.
Spare	Pin 4	n.c.
PC_CONNECT +	Pin 5	3
PC_CONNECT -	Pin 6	4
CIRCUIT QUENCH LOOP +	Pin 7	5
CIRCUIT QUENCH LOOP -	Pin 8	6
POWERING PERMIT_LOOP_B2 +	Pin 9	7
POWERING PERMIT_LOOP_B2 –	Pin 10	8
POWERING PERMIT_LOOP_B1 +	Pin 11	9
POWERING PERMIT_LOOP_B1 –	Pin 12	10

Hardware Interface Type C– Cable ID: C-PIC-PC

For up to four power converters in one rack, an 18-wire cable (NE18) with a Burndy 19 pin connector at each end has been selected between the PIC and the rack. The type of the connector at then end of the cable is a 19 male poles Burndy connector, type 19BPMB, with the following pin assignment:

Name	**PC or PIC side**	**NE18 Wire**
Circuit 1.1 POWERING PERMIT LOOP +	Pin 1	1
Circuit 1.1 POWERING PERMIT LOOP -	Pin 2	2
Circuit 1.1 POWERING FAILURE LOOP +	Pin 3	3
Circuit 1.1 POWERING FAILURE LOOP -	Pin 4	4
Circuit 1.2 POWERING PERMIT LOOP +	Pin 5	5
Circuit 1.2 POWERING PERMIT LOOP -	Pin 6	6
Circuit 1.2 POWERING FAILURE LOOP +	Pin 7	7
Circuit 1.2 POWERING FAILURE LOOP -	Pin 8	8
Circuit 2.1 POWERING PERMIT LOOP +	Pin 9	9
Circuit 2.1 POWERING PERMIT LOOP -	Pin 10	10
Circuit 2.1 POWERING FAILURE LOOP +	Pin 11	11
Circuit 2.1 POWERING FAILURE LOOP -	Pin 12	12
Circuit 2.2 POWERING PERMIT LOOP +	Pin 13	13
Circuit 2.2 POWERING PERMIT LOOP -	Pin 14	14
Circuit 2.2 POWERING FAILURE LOOP +	Pin 15	15
Circuit 2.2 POWERING FAILURE LOOP -	Pin 16	16
PC_CONNECT +	Pin 17	17
PC_CONNECT -	Pin 18	18
Spare	Pin 19	n.c.

Appendix B: Cables between PIC and QPS

Ground connection: it is required to always connect both sides of the cable shielding ("tresse") to minimise possible electromagnetic interference.

The cable is identical for interface type A1 and A2. A 6-wire cable (NE6) has been chosen for the interface between QPS and PIC for each circuit. The type of the connector at each end is an 8 male poles Burndy connector, type 8BPMB (6 poles is not existing) with the following pin assignment:

Hardware Interface Type A – Cable ID: A-PIC-QPS

Name	**PIC or QPS side**	**NE 6 Wire**
CIRCUIT QUENCH LOOP +	Pin 1	1
CIRCUIT QUENCH LOOP -	Pin 2	2
DISCHARGE LOOP +	Pin 3	3
DISCHARGE LOOP -	Pin 4	4
Spare	Pin 5	n.c.
Spare	Pin 6	n.c.
QPS_CONNECT +	Pin 7	5
QPS_CONNECT -	Pin 8	6

Hardware Interface Type B – Cable ID: B-PIC-QPS

For a module with up to four quench detectors, a 10-wire cable (NE10) has been chosen to interface it with the PIC for both, interface type B1 and B2. The maximum number of detectors for this interface is four, but it is possible that less than four detectors are installed. The type of the connector at each end is a 12 male poles Burndy connector, type 12BPMB with the following pin assignment:

Name	PIC or QPS side	NE 10 Wire
Circuit 1 CIRCUIT QUENCH LOOP +	Pin 1	1
Circuit 1 CIRCUIT QUENCH LOOP -	Pin 2	2
Circuit 2 CIRCUIT QUENCH LOOP +	Pin 3	3
Circuit 2 CIRCUIT QUENCH LOOP -	Pin 4	4
Circuit 3 CIRCUIT QUENCH LOOP +	Pin 5	5
Circuit 3 CIRCUIT QUENCH LOOP -	Pin 6	6
Circuit 4 CIRCUIT QUENCH LOOP +	Pin 7	7
Circuit 4 CIRCUIT QUENCH LOOP -	Pin 8	8
Spare	Pin 9	n.c.
Spare	Pin 10	n.c.
QPS_CONNECT +	Pin 11	9
QPS_CONNECT -	Pin 12	10

Appendix C

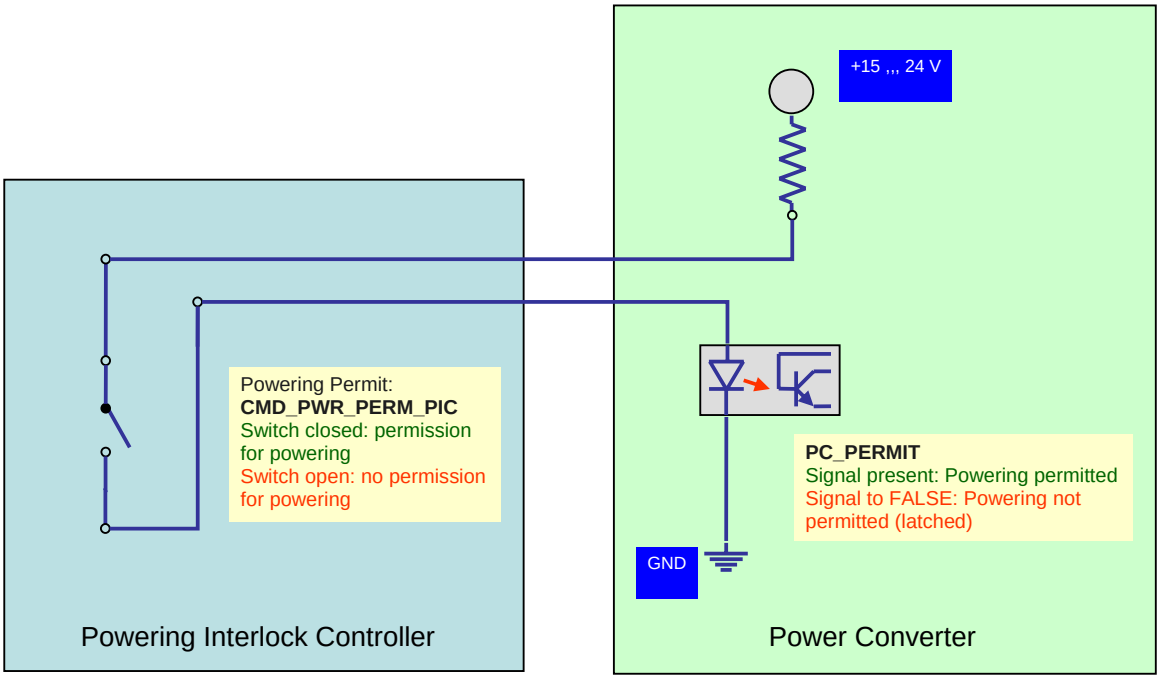


Figure 4: Powering Permit LOOP

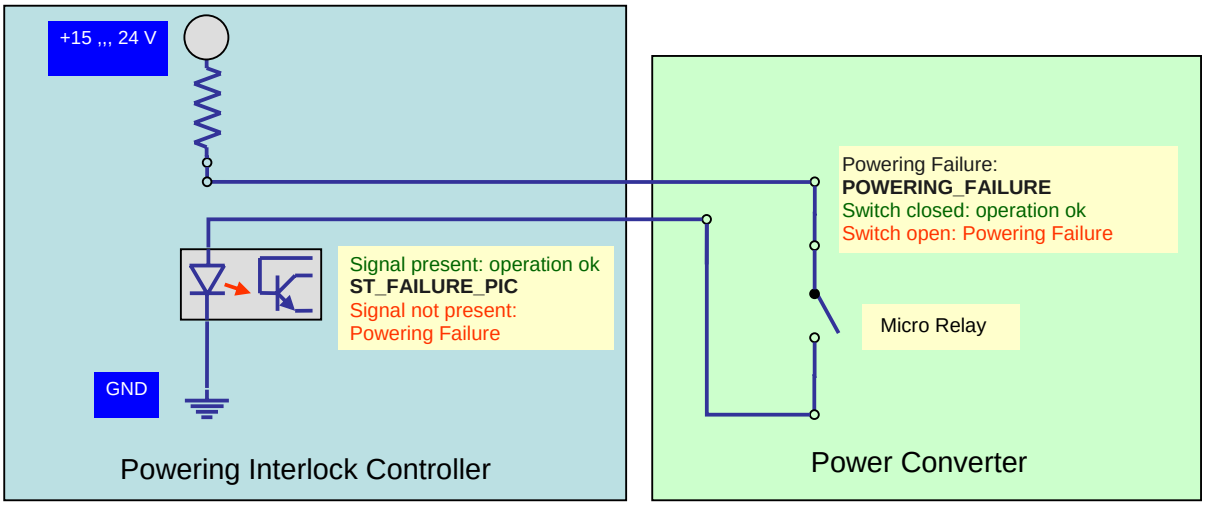
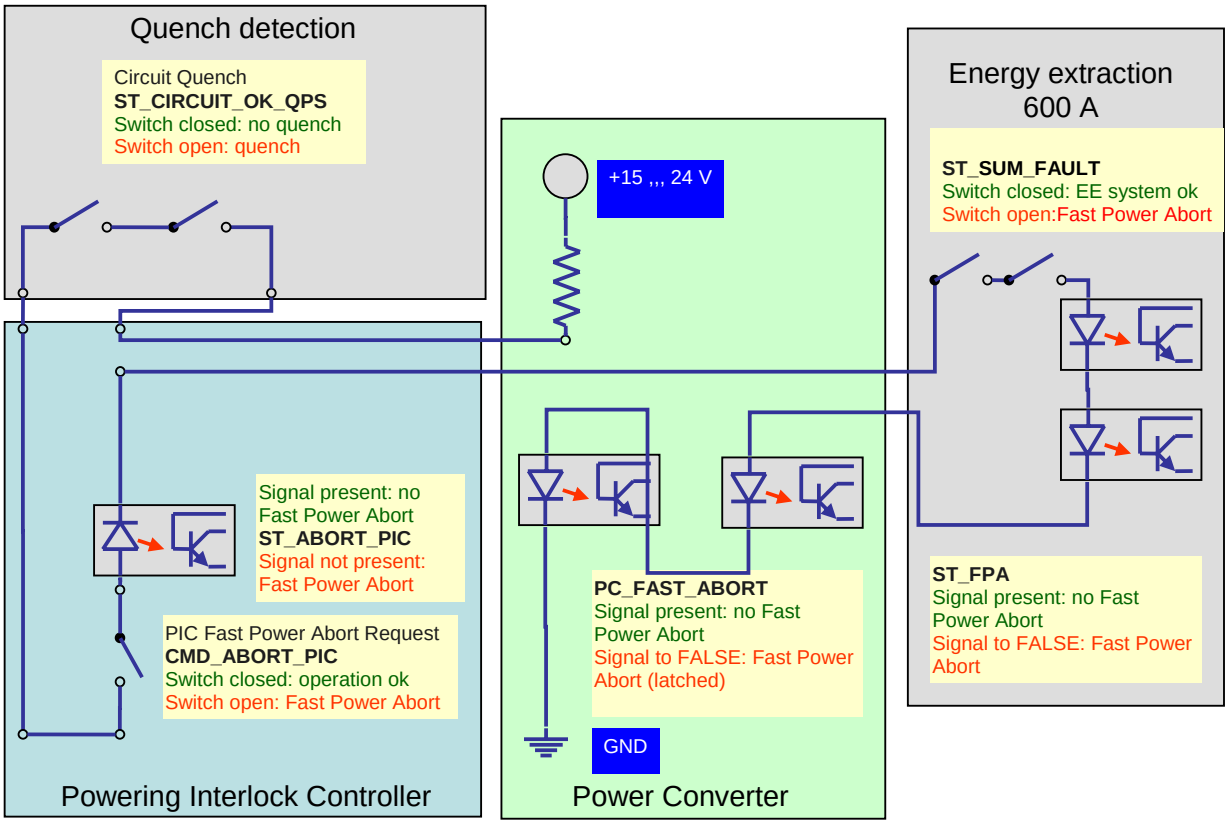


Figure 5: Powering Failure LOOP

Note: The given names for power converter signals relate to the name on the hardware level. See Appendix H for correspondence with signals published via the FGC



Note: The connection with the energy extraction system is internal to the converter and not seen by the PIC (EE rack and power converter are back to back). If there is no external energy extraction system in the circuit, the connection is short-circuited at the power converter level.

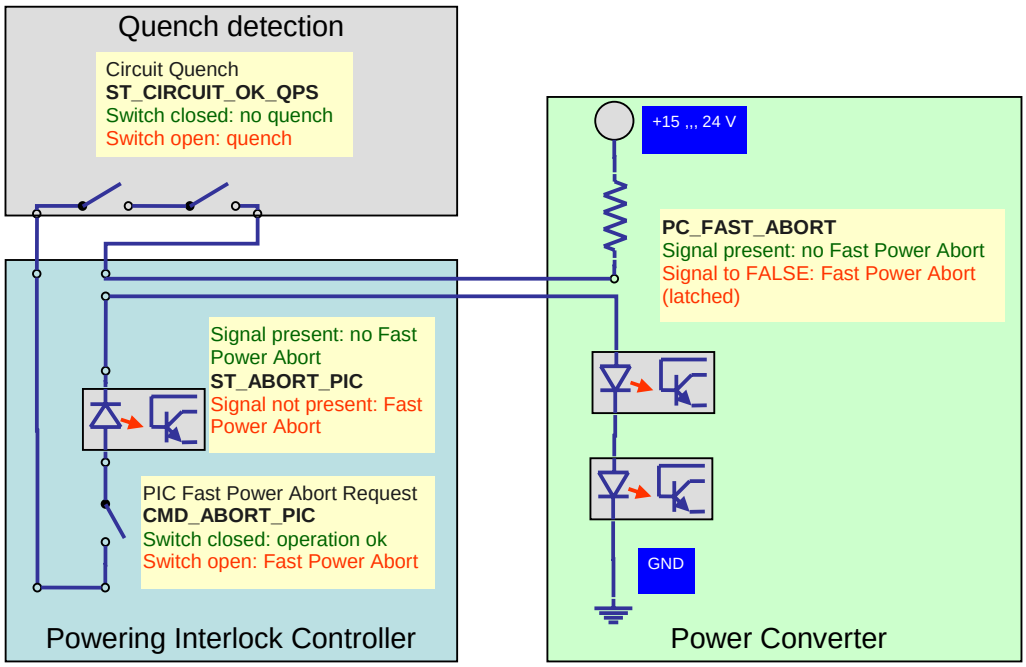


Figure 6: Circuit Quench LOOP with and without energy extraction system (the figure below applies also to the 13kA circuits having there EE system directly in the local QPS loop)

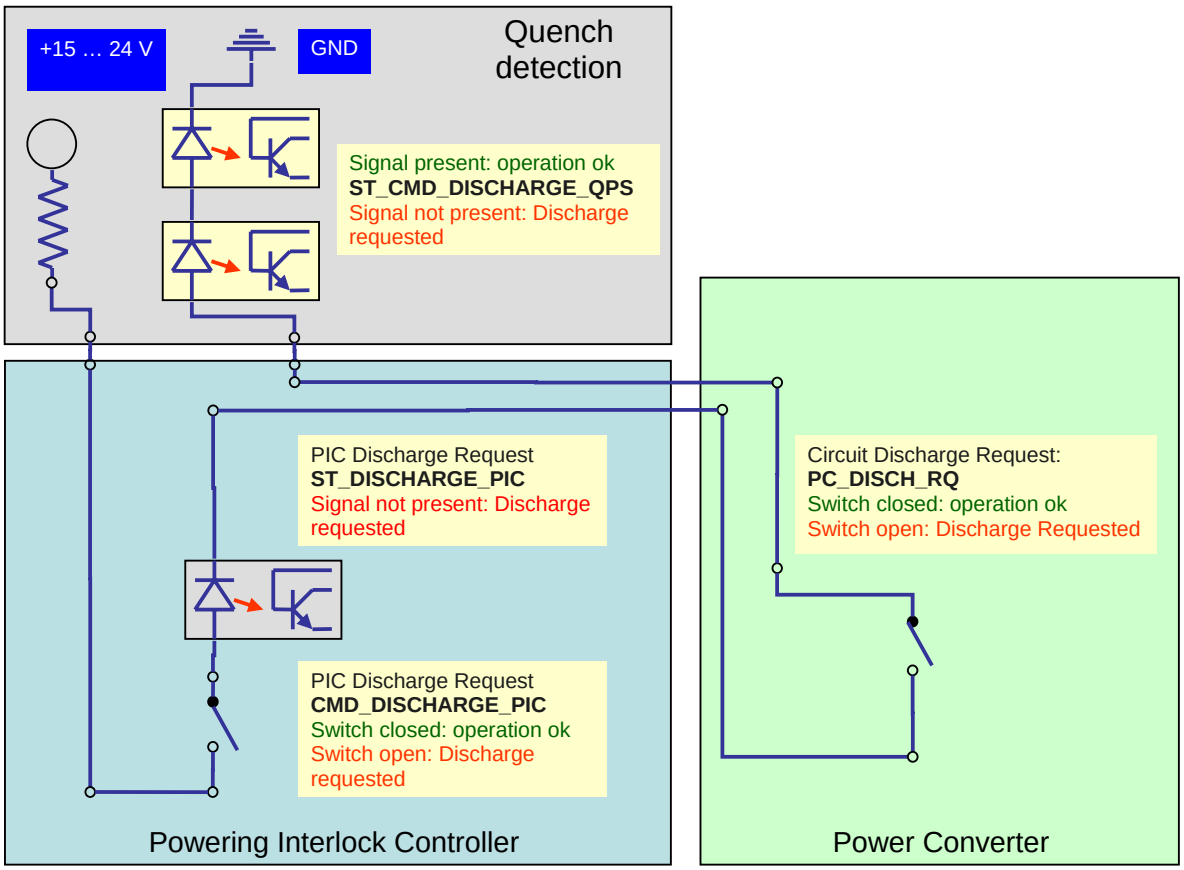


Figure 7: Discharge LOOP

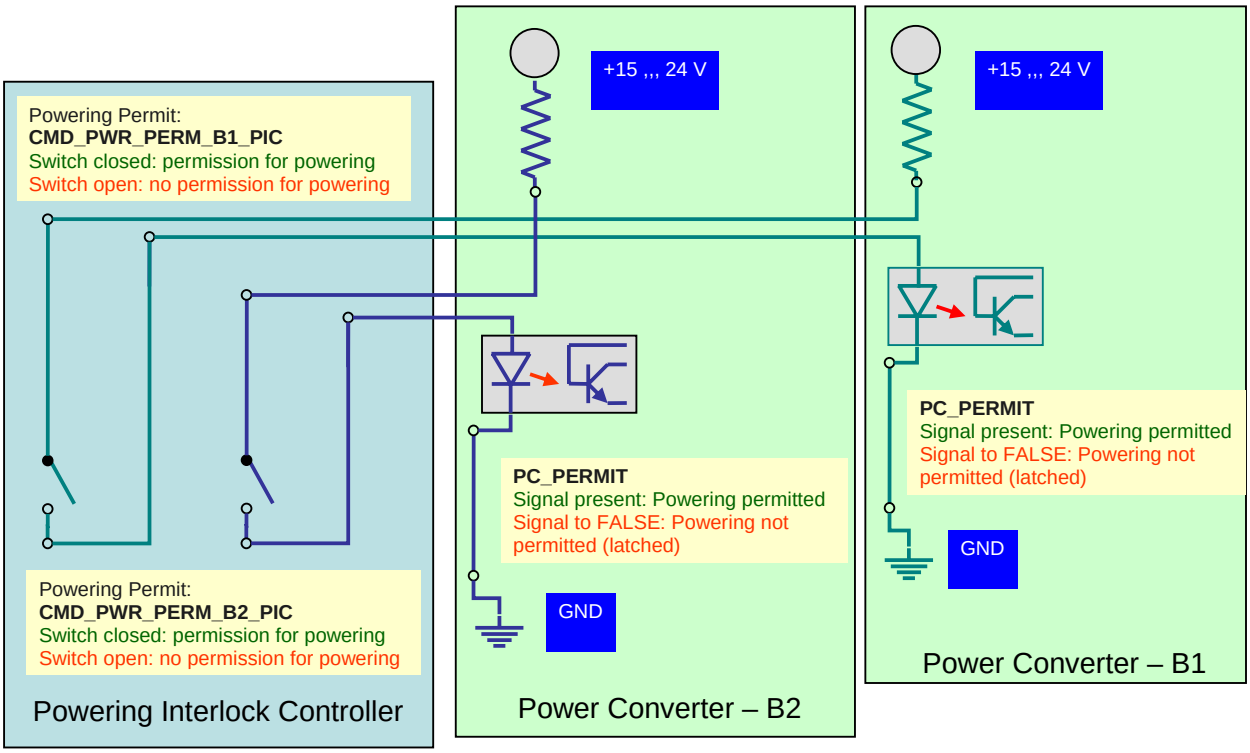


Figure 8: Powering Permit LOOP for MQM/MQY configurations

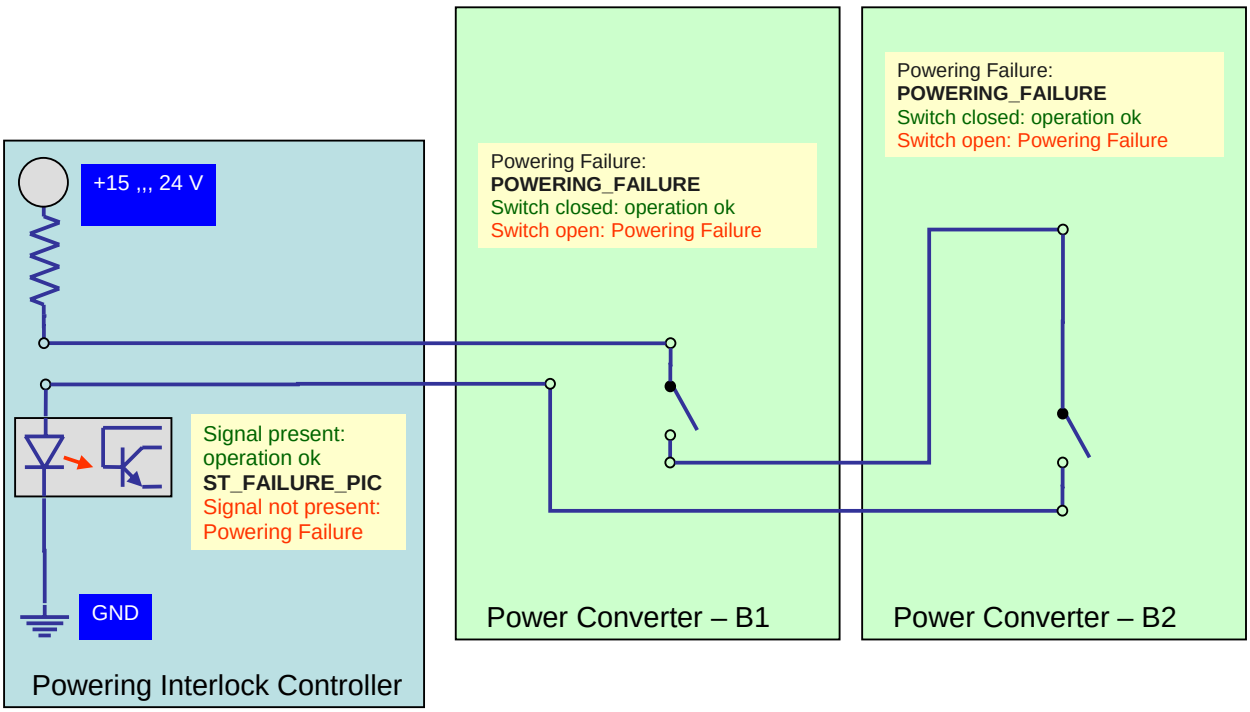


Figure 9: Powering Failure LOOP for MQM/MQY configurations

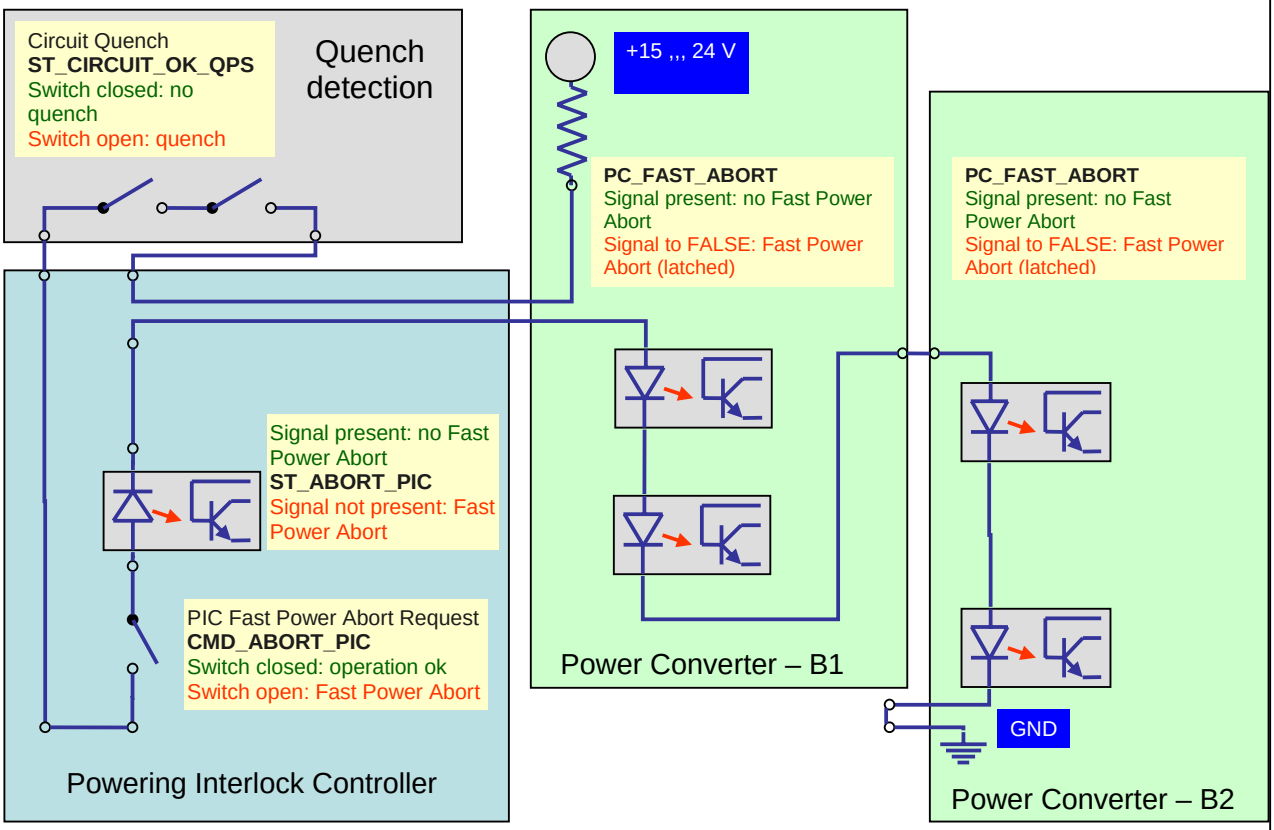


Figure 10: Circuit Quench LOOP for MQM/MQY configurations

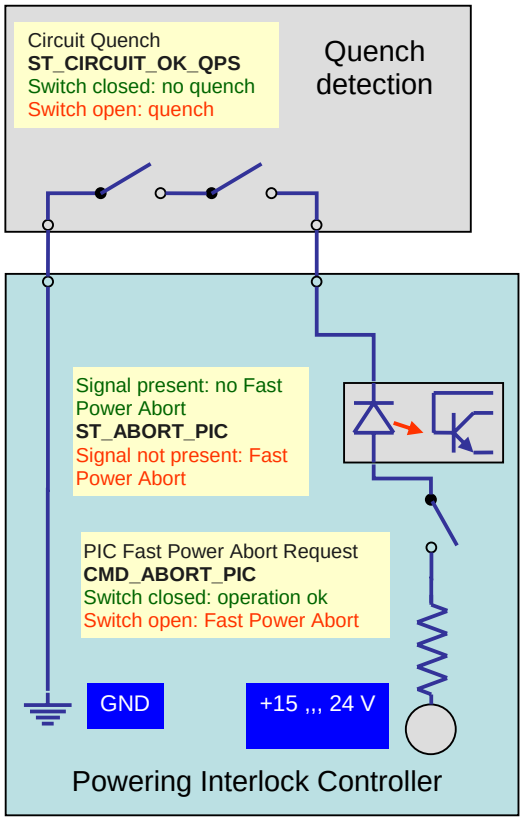


Figure 11: Circuit Quench LOOP for main dipole circuits in the odd points (the switch in the PIC is proposed for standardisation, but not required for the functionality)

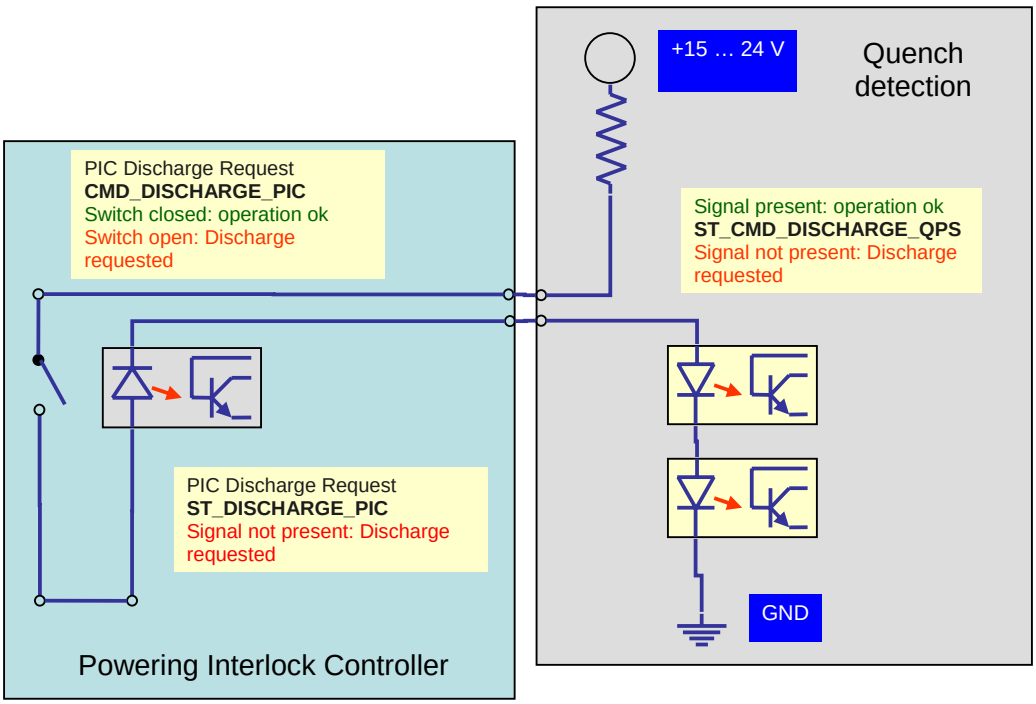


Figure 12: Discharge LOOP for main dipole circuits in the odd points

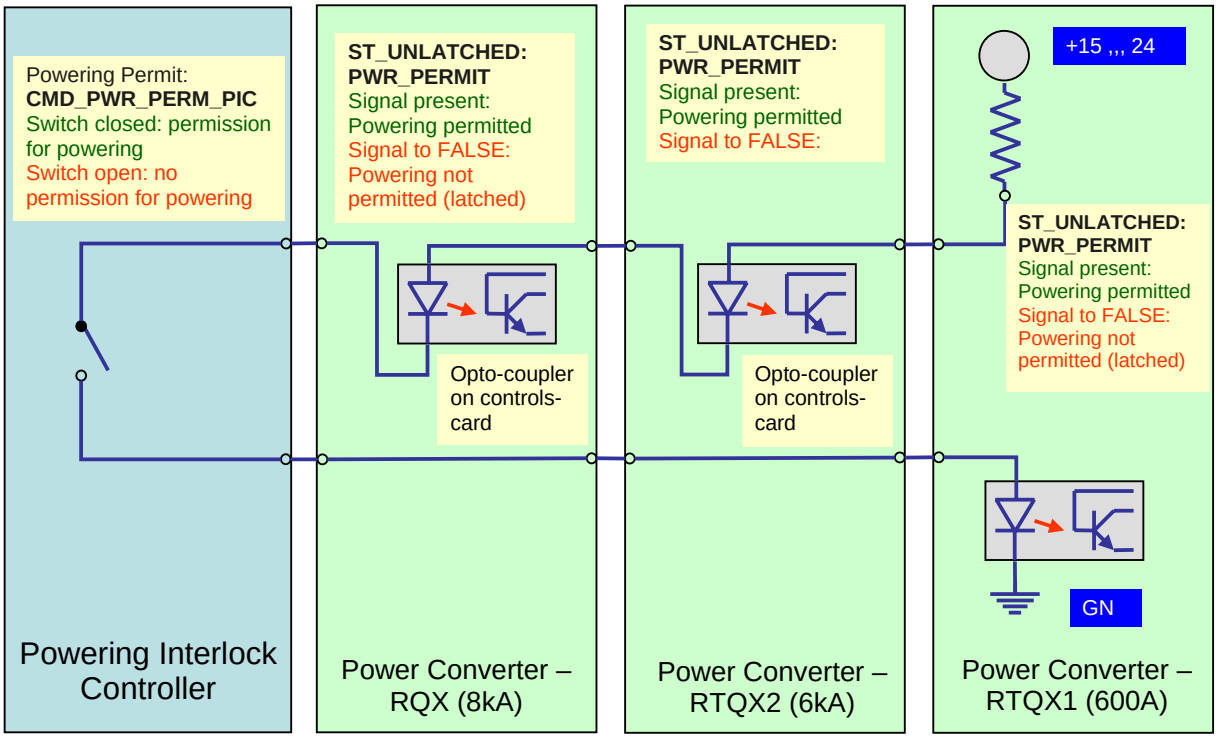


Figure 13: Powering Permit LOOP for inner triplet configuration

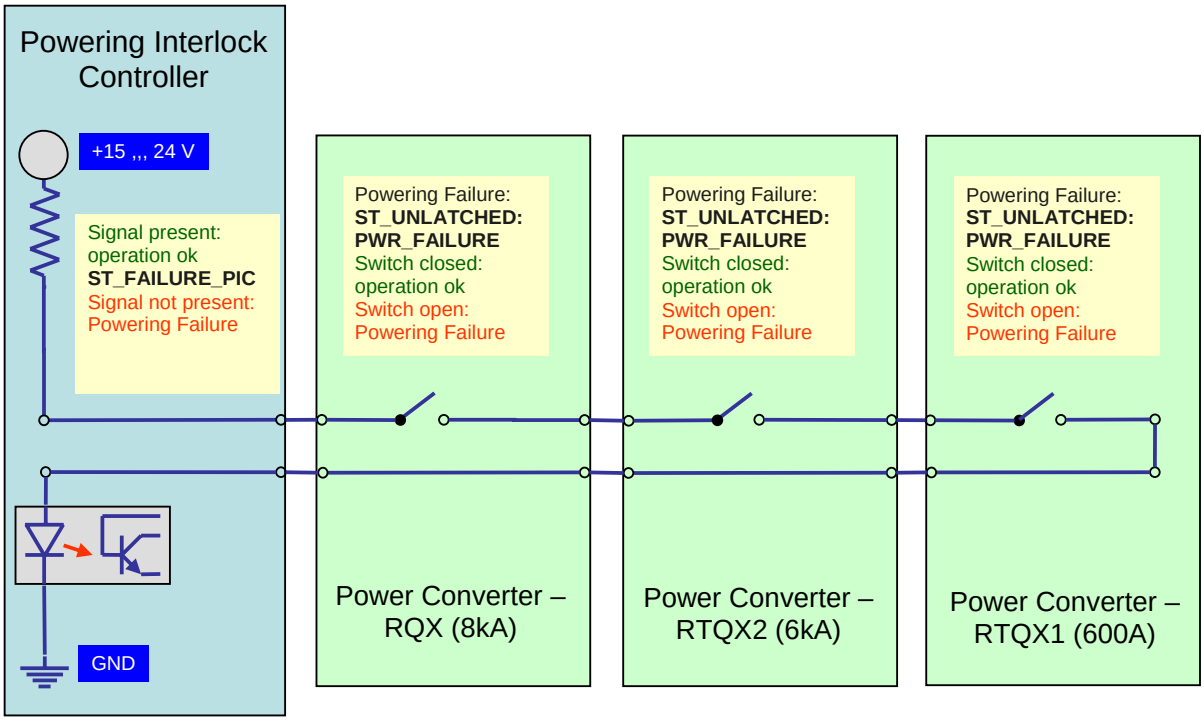


Figure 14: Powering Failure LOOP for inner triplet configuration

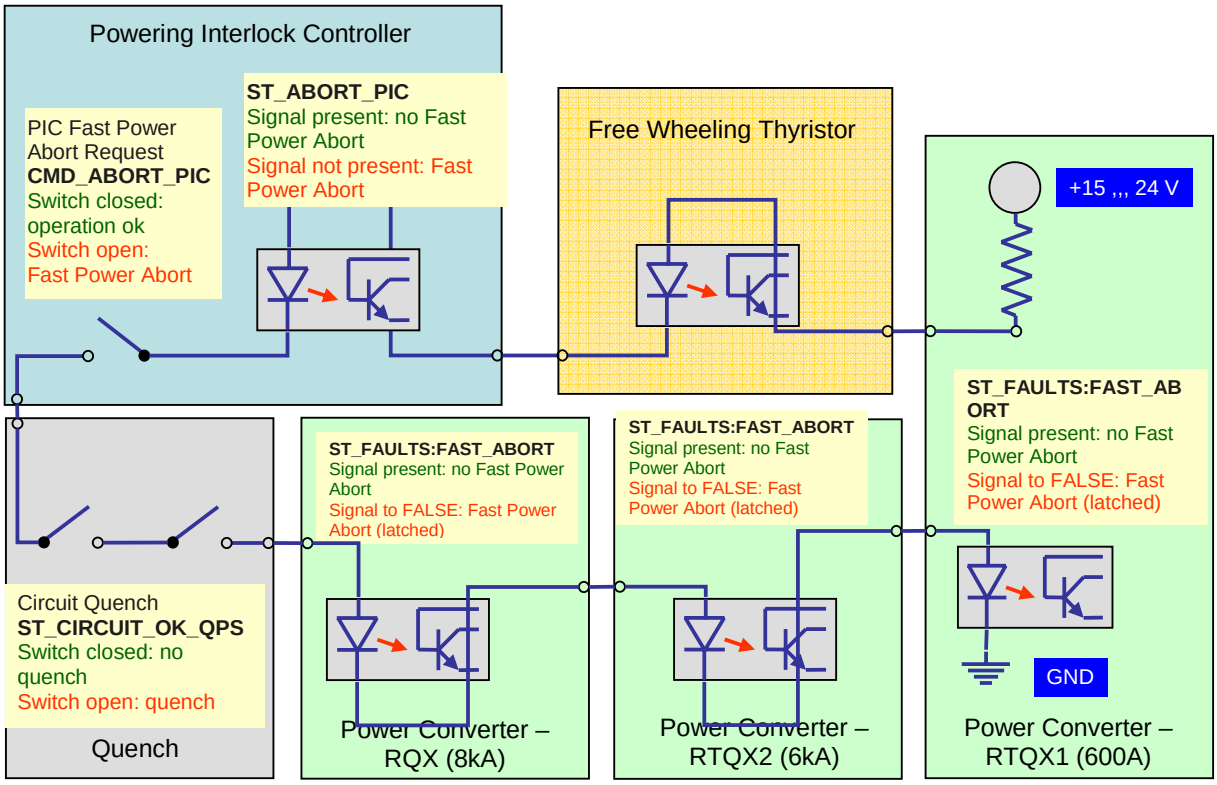


Figure 15: Quench LOOP for inner triplet configuration

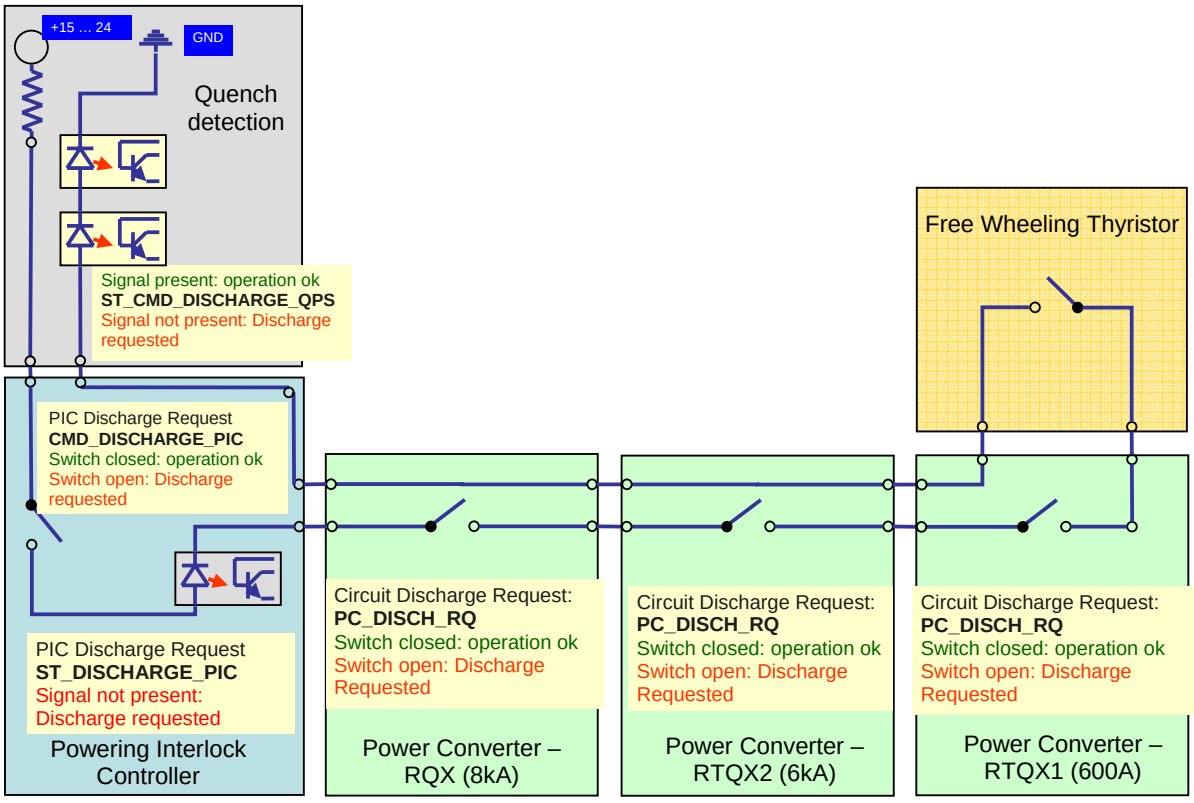


Figure 16: Discharge LOOP for inner triplet configuration

APPENDIX D

Circuit types	I ultimate [kA]	No. of Interfaces for circuits in the LHC	Interface Type
RB (even IP's)	13	8	A1
RB (odd IP's)	13	8	A2
Arc RQF, RQD	13	16	A1
RQX (including RTQX2 and RTQX1)	0.6 – 12	8	A1
Insertion RQ using MQM/MQY	3.9 – 5.8	78	B2
RD1.R(L)2(8), RD2.R(L)1,2,5,8, RD3.R(L)4, RD4.R(L)4	4.6 – 6.2	16	B1
RCD, RCS, ROD, ROF, RQS, RQTD, RQTF, RQTL9, RSD, RSF, RSS, RQT, RQTL, RQ6.R(L)3(7), RCBC (only R3)	0.6	346	B1
RCBX, RQSX, RCO, RU	0.6	74	B1
RCBC (except R3), RCBY	0.08 – 0.12	234	C
RCOSX, RCOX, RCSSX3, RCSX3, RCTX3	0.06 – 0.12	40	C
RCBV(H)	0.06	752	D

Table 3: Interfaces for different Types of Electrical Circuits

Interface Type	I ult [kA]	General Power Abort	Discharge after General PA	After Discharge Request or Quench		Essential for beam	Examples
				Resistor	Fire Heaters		
A1, A2	13	YES	FAST	YES	NO	1	RB, RQF, RQD
A1	13	YES	FAST	NO	YES	1	RQX
B2	6.2	YES	FAST	NO	YES	1	Insertion RQ
B1	6.2	YES	FAST	NO	NO	1	RD
B1	0.6	NO	FAST	YES	NO	1	RQT, RSF, RSD
B1	0.6	NO	FAST	NO	NO	0	RCO, RCBX
C	0.12	NO	SLOW	NO	NO	0	RCBC, RCBY
C	0.12	NO	SLOW	NO	NO	0	RCOSX, RCOX

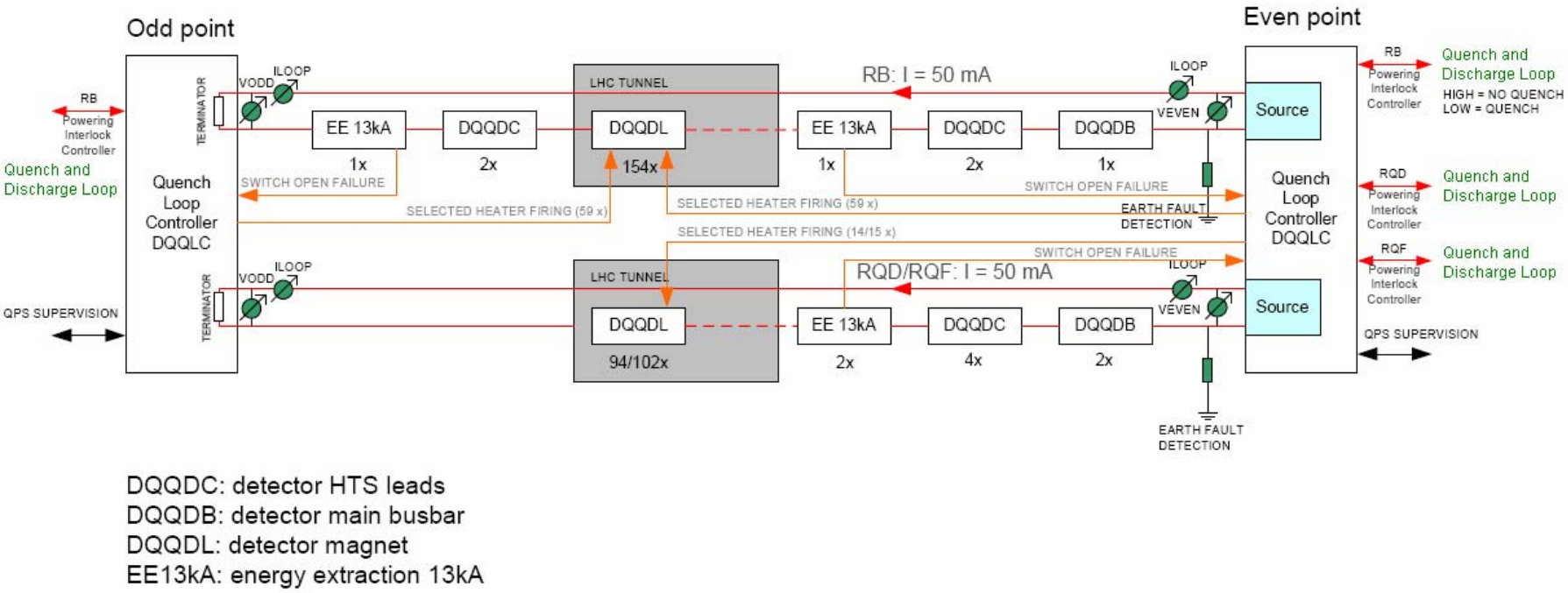
Table 4: Features of the different Interfaces and suggested values for Circuit Variables

APPENDIX E

	Hardware Loops between PIC and PC						HW Loops between PIC and QPS				
Hardware Interface Type	PC Connect	Powering Failure	Discharge	Powering Permit I	Powering Permit II	Circuit Quench	QPS Connect	Circuit Quench	Discharge	Powering Subsector OFF	Essential for beam
A1	YES	YES	YES	YES	NO	YES	YES	YES	YES	YES	YES
A2	NO	NO	NO	NO	NO	NO	YES	YES	YES	YES	YES
B1	YES	YES	NO	YES	NO	YES	YES	YES	NO	NO	YES
B1	YES	YES	NO	YES	NO	YES	YES	YES	NO	NO	NO
B2	YES	YES	NO	YES	YES	YES	YES	YES	NO	YES	YES
C	YES	YES	NO	YES	NO	NO	NO	NO	NO	NO	YES
C	YES	YES	NO	YES	NO	NO	NO	NO	NO	NO	NO
D	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO	NO

Table 5: Interface Types and suggested values for Circuit Variables

APPENDIX F



DQQDC: detector HTS leads
DQQDB: detector main busbar
DQQDL: detector magnet
EE13kA: energy extraction 13kA

Figure 17: Interfaces of Powering Interlock Controller with the QPS system for the main dipole and quadrupole circuits of a long arc cryostat.

Note that the QPS system is also using current loops stretching along the 3km long arc, which will connect all local quench detector units of the magnets, busbars and current leads. The interface towards the powering interlock controller (namely the quench and discharge loop) is provided by the Quench loop controller in the even side (for RB, RQD, RQF circuits) and in addition the odd side for the RB circuit.

APPENDIX G

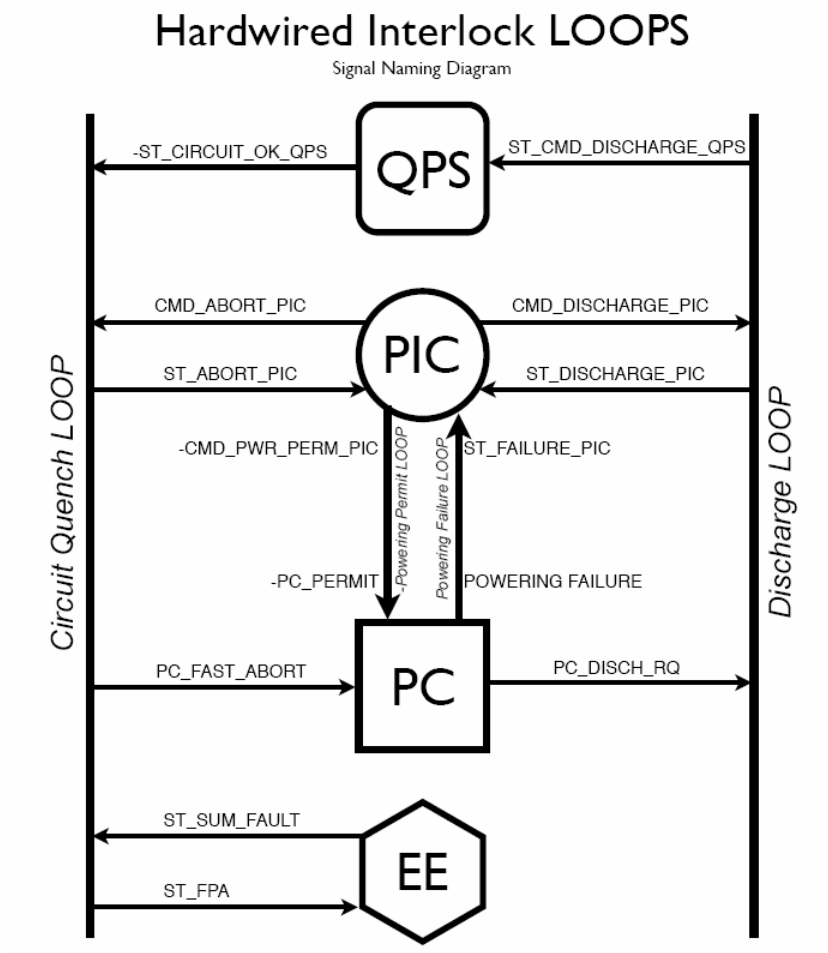


Figure 18: Interfaces of interlocked equipment with the Powering Interlock Controller via the quench and discharge loop for circuit type A.

APPENDIX H

Signal name used by voltage source electronics	Signal name used by CERN electronics (FGC)	Name of software property published by the FGC	Input / Output	Description
PC_FAST_ABORT		ST_FAULTS:FAST_ABORT	Input	The contact PC_FAST_ABORT (Fast Power Abort) is open if the Interlock System orders the voltage source to switch off immediately. The contact is otherwise closed.
PC_DISCH_RQ		ST_UNLATCHED:PC_DISCH_RQ	Output	The contact PC_DISCH_RQ (Discharge Request) is open if the converter asks the Interlock System to open the energy extraction switches. The contact is otherwise closed.
PC_CONNECT			Output	The contact PC_CONNECT shall always be closed by the voltage source. This signal is used by the Interlock System to know if the cable between the converter and the Interlock System is connected.
	PC_PERMIT	ST_UNLATCHED:PC_PERMIT	Input	The contact PC_PERMIT (Power Permit) is open if the Interlock System orders the voltage source to switch off smoothly. The contact is otherwise closed.
	POWERING_FAILURE	ST_UNLATCHED:PWR_FAILURE	Output	The POWERING_FAILURE contact is open if a fault is detected on the Power Converter. The contact is otherwise closed.

Table 6: Correspondence table for hardware signals and software properties of power converters (extracted from LHC Project documentation LHC-RPH-CI-0001)

The signal definitions for power converters cannot be found in the naming database down to the bit level, but are available in documentation of the published data of the FGC2 Class 51 [4].